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Semiconductor Measurement Technology:

Method to Determine the Quality of Sapphire

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Method to Determine the Quality of Sapphire

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PREFACE

This study was carried out at the RCA Laboratories as a part of the Semiconductor Technology Program in the Electronic Technology Division at the National Bureau of Standards. The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce, and for use by industry in controlling device fabrication processes.

This research was funded by the Defense Advanced Research Projects Agency, Order 2397, through the National Bureau of Standards' Semiconductor Technology Program, Contract 5-35915. The contract was monitored by K. F. Galloway as the Contracting Officer's Technical Representative.

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Semiconductor Measurement Technology:
METHOD TO DETERMINE THE QUALITY OF SAPPHIRE

by

M. T. Duffy, P. J. Zanzucchi, W. E. Ham,
J. F. Corboy, and G. W. Cullen

Abstract: Specular reflectance measurements were used in the quantitative characterization of sapphire and silicon surfaces. Residual polishing damage in sapphire surfaces can be easily detected by infrared multiple reflectance measurements in the lattice-band region of sapphire, nominally 300 to 900 cm^{-1}. Specular reflectance measurements in the ultraviolet, at a photon energy of 4.3 eV (corresponding to the $X_4 - X_1$ silicon transition), have been used for the surface characterization of bulk silicon surfaces and silicon films on sapphire. This measurement is sensitive to crystalline quality, polishing damage, and surface texture which cause light-scattering effects. The reflectance methods are fast, nondestructive, and can be used for quality control and research purposes.

The reflectance methods were applied to the characterization of variously polished sapphire surfaces and to the characterization of heteroepitaxial silicon films grown on the substrates. The results of these measurements were correlated with various parameters of silicon-on-sapphire (SOS) devices fabricated in the silicon films. Measured device parameters include drain current, extrapolated threshold voltage, leakage current, and drain breakdown voltage. Most device data were automatically recorded using a special device test pattern and simple statistical data were computed for the various device parameters.

Key Words: Infrared reflectance, optical reflectance, polishing, silicon on sapphire, surface roughness, ultraviolet reflectance, work damage.

1. INTRODUCTION

The purpose of this program was to develop fast, nondestructive optical testing methods for determining the surface quality of sapphire substrates and heteroepitaxial silicon films grown on these substrates. The program also included the correlation of optical data with data from

conventional analytical techniques and with the electrical properties of heteroepitaxial silicon films in silicon-on-sapphire (SOS) structures, including discrete device performance.

It is generally accepted that the crystalline perfection of homoepitaxial and heteroepitaxial layers is strongly influenced by the crystalline perfection of the substrate surface. It is well known from studies on the homoepitaxial growth of silicon that defects on the substrate surface lead to crystal growth defects in the epitaxial layer [1,2].* It has also been shown by the use of Lang topographic x-ray techniques that the crystalline perfection of heteroepitaxial III-V compounds on both sapphire and spinel substrates is significantly altered by defects on the substrate surface [3]. These defects are often introduced in the polishing process and may not be visible microscopically prior to epitaxy. The heteroepitaxial layer above such defects may be misoriented with respect to the rest of the layer, thus introducing lattice imperfections in the layer. Similar effects in silicon-on-sapphire structures can lead to enhanced diffusion rates in the defect region in the silicon [4]. Several electronic materials are prepared epitaxially by chemical vapor deposition for a variety of applications, and there is a need for fast, nondestructive, and quantitative measurement techniques for determining substrate surface quality and epitaxial film quality.

Until recently, quality control procedures for the inspection of sapphire substrates and heteroepitaxial silicon films have relied on visual inspection and microscopic examination at low magnification. These methods are inadequate for quantitatively describing such properties as substrate surface polishing damage (which influences heteroepitaxial growth), heteroepitaxial silicon crystalline quality (which affects device performance), and film surface texture or "haze," which has been subjectively used as the basis for accepting or rejecting samples from the product line by visual inspection. Because of the lack of quantitative data, it is usually difficult to find a correlation between device performance and initial material properties as determined by the preparative parameters. It should be noted, however, that there are many factors other than the preparative parameters which influence discrete device performance and yield.

The work performed in this program provides a basis for the rapid quantitative characterization of sapphire substrates and heteroepitaxial silicon films by specular reflectance measurements. The methods used are fast, nondestructive, require no contact to the sample surface, and are suitable for in-line quality control and research purposes.

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*Figures in brackets indicate literature references at the end of this publication.

In principle, the methods are applicable to systems other than silicon on sapphire.

Specifically, sapphire substrate surface damage, resulting from cutting and polishing procedures, can be detected by infrared specular reflectance measurements in the lattice-band spectral region of sapphire. This will be explained in the next section. The crystalline quality of heteroepitaxial silicon films on sapphire can be determined by specular reflectance measurements in the ultraviolet at a photon energy of about 4.3 eV (corresponding to the X_4-X_1 silicon transition). This will also be explained in the next section.

Correlation of reflectance data with data from conventional analytical techniques involved the use of x-ray analysis, optical microscopy, scanning electron microscopy, and electrical measurements. The application of these techniques will be described later in the text.

Correlation of the surface quality of the starting materials (sapphire substrates and heteroepitaxial silicon films) with discrete device performance is an important part of this study. The test structure used in device fabrication has been described previously [5]. The test pattern arrangement permits the evaluation of many similar devices, both n- and p-channel transistors, across a given wafer. A range of polishing damage was intentionally introduced in the sapphire substrates and measured by infrared reflectance. Some substrates were annealed prior to silicon heteroepitaxy. Silicon films were evaluated by ultraviolet reflectance measurements. Data from both measurements were correlated with data obtained in device measurements. Analysis of the results gives information on the relationship between substrate polishing variables and the quality of heteroepitaxial silicon films as related to discrete device performance.

A limitation of these reflectance measurement methods is that a relatively large surface area is monitored in comparison to the area of an SOS device. Thus, localized defect areas are not likely to be detected unless the density of such defects is high enough to cause noticeable changes in reflectance. Nevertheless, the reflectance measurements are very useful for quickly determining average surface crystalline quality.

2. PROCEDURE

Historically, many quantitative optical testing methods (see, e.g., bibliography of various optical testing methods reported by D. Malacara et al. [6]) are available, well known, and widely used. In particular, variations of the Tolansky techniques involving multiple-beam interferometry have been and are still widely used to measure surface contours or surface flatness. However, these techniques do not determine the degree of lattice damage beneath a polished surface. Since the epitaxial process involves oriented crystal growth which is initiated by the crystallographic characteristics of the substrate surface, information concerning lattice damage is also needed to characterize more fully the properties of substrate surfaces.

To develop a practical, nondestructive optical method for testing the surface quality of sapphire substrates, we have extended the previously published work of A. S. Barker, Jr. [7]. His work shows that polishing procedures affect the degree of lattice-related strain present at the sapphire surface. This strain deforms the normal modes for the single-crystal aluminum oxide (sapphire) vibrational states and gives rise to forbidden modes in the specular reflection spectrum. In this technique, substrate surface damage is correlated, quantitatively, with changes in the specular reflectance spectrum and in the optical constants of the sapphire surface in the lattice-band region, nominally 300 to 900 cm^{-1}. A detailed description of this technique as developed for the present program can be found in references [8-10].

Briefly, the optical constants of variously polished sapphire substrates were calculated from specular reflectance data using Kramers-Kronig analysis [11-13]. A computer program by Klucker and Nielsen [12] was used to calculate values of n and k, the refractive index and absorption index, respectively. Complementary notes on the computer program are given in reference [9]. From a knowledge of the optical constants it was possible to determine which vibrational modes of sapphire were most affected by surface polishing damage. It was determined that substrate surface damage, resulting from cutting and polishing procedures, can be readily detected by multiple specular reflectance measurements in the sapphire lattice-band region at wavenumber 600 cm^{-1}. Multiple reflectance measurements greatly enhance the sensitivity of the method. It is important, however, that substrates are not annealed prior to this measurement; otherwise, the strain induced by polishing damage is relieved, and the substrate

surface gives a spectrum similar to damage-free sapphire. In practice, the measurement of absolute intensity is subject to errors due to substrate curvature, misalignment of the optics, and surface cleanliness. For practical applications, the ratio, $I_{600\ cm^{-1}}/I_{450\ cm^{-1}}$, from multiple reflectance measurements was used to represent, quantitatively, substrate surface damage (where $I_{600\ cm^{-1}}$ represents the reflected intensity at wavenumber 600 cm^{-1}, and $I_{450\ cm^{-1}}$ the corresponding value at 450 cm^{-1}). Thus, measurements at two wavelengths are required. The value of $I_{450\ cm^{-1}}$ is much less sensitive to surface damage than the value of $I_{600\ cm^{-1}}$. Thus, the above ratio is very helpful in minimizing measurement errors. Figures 6 and 7 of reference [10] show the multiple reflectance spectrum for a damage-free and damaged sapphire substrate [$(1\bar{1}02)$-oriented], respectively. The influence of surface damage on the reflected intensity at 600 cm^{-1} is clearly demonstrated.

The crystalline quality of silicon can also be determined by optical reflectance measurements. Kühl et al. [14] have shown differences in the optical constants of epitaxial, polycrystalline, and amorphous silicon in the energy range 0.5 to 5.5 eV. Their work indicates that the X_4-X_1 silicon transition at 4.3 eV is strongly influenced by crystalline character. Donovan et al. [15] have shown that the optical reflectance of variously polished germanium surfaces is affected by residual surface damage. In this program, the specular reflectance, R, of the silicon films, measured (in the ultraviolet region) at a photon energy of 4.3 eV (corresponding to the X_4-X_1 silicon transition) was used to determine heteroepitaxial film quality. The reflectance values were expressed, logarithmically, relative to the reflectance (R_o) of an aluminum surface mirror, i.e., log (R_o/R). This procedure was used in the surface evaluation of a set of silicon substrates which had a wide range of polishing damage. Reflectance data from the set of silicon substrates were then arbitrarily used as a basis of comparison for demonstrating the quality of heteroepitaxial silicon films on sapphire. These measurements have been described previously [16,17]. In the optical characterization of heteroepitaxial silicon, surface texture or "haze" also influences the reflected intensity because of light-scattering effects. Thus, the reflected intensity from silicon films, as described above, is influenced by both crystalline quality and surface texture. There is evidence to indicate that poor crystallinity is very often accompanied by enhanced surface texture and

light-scattering. However, it is not clear that this is true in all cases. Accordingly, it would be of interest to separate these two effects.

Various theories and methods have been developed for determining changes in reflectance due to light-scattering effects and plasmon excitation on thin metal films deposited on different substrates (see, e.g., Bennett and Porteus [18], Endriz and Spicer [19], Cunningham and Braundmeier [20], and Bennett [21], for methodology and bibliography). None of these methods is directly applicable to silicon on sapphire without prior surface metallization, which is impractical for quality control purposes, though it is of research interest. In preliminary work in this program, the rms surface roughness (σ) of variously polished silicon substrates has been obtained by the method of Cunningham and Braundmeier [20] (see ref. [17]). This parameter, in turn, can be correlated with the polishing grit size and with the optical reflectance data for the damaged silicon substrates. The reflectance of silicon on sapphire can then be compared with the reflectance data for the silicon substrates as indicated above. This, however, does not give a measure of the surface roughness of silicon on sapphire, but merely a basis for comparison.

Correlation of reflectance data with data from conventional analytical measurement techniques involved the use of x-ray analysis (line-broadening, twinning concentration, and x-ray topography), optical microscopy, scanning electron microscopy, and electrical measurements (Hall mobility and gated-Hall mobility). Since these measurement techniques required no special development for this program, further discussion will be deferred to the next section.

Correlation of surface quality (of sapphire substrates and heteroepitaxial silicon films) with discrete device performance involved the preparation of sapphire substrates with a wide range of polishing damage. This was accomplished by either using diamond grit in the final surface finishing of substrates or by damaging well-polished surfaces with diamond grit. Both approaches gave similar results. The grit size ranged from 0.1 μm to 6 μm, and the best surfaces were prepared by polishing with silica sol.

The range of surface damage is best illustrated by referring to figure 1, which is a plot of the infrared multiple reflectance ratio, $I_{600\ cm^{-1}}/I_{450\ cm^{-1}}$, vs polishing grit size. The reflectance ratio ranges from about 0 to 1, representing the worst and best surfaces. On this scale, 0 represents surface finishing with 6-μm-diamond (the worst surface). There is some difficulty in preparing substrate surfaces represented by points on the steep part of the curve. Even

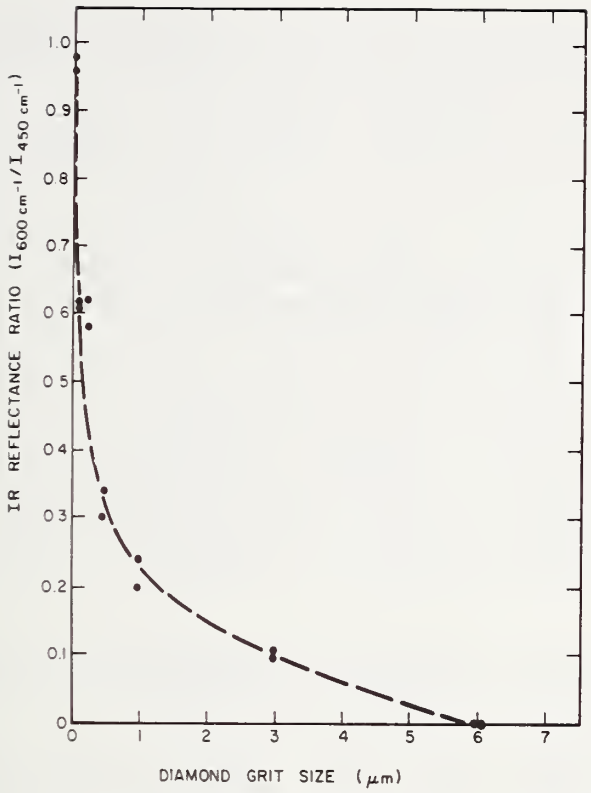

Figure 1. Dependence of infrared reflectance ratio for variously polished sapphire substrates, on polishing grit (diamond) size.

0.1-μm-diamond finish can produce much more degraded surfaces than shown in figure 1 if polishing is continued for prolonged periods. To obtain surfaces characteristic of data points on the steep part of the curve, a nonreproducible trial and error process is necessary, with reflectance monitoring necessary every two or three minutes, to obtain the desired range of damage. On the other hand, this level of damage may occur, inadvertently, in the surface finishing of commercial substrates if quality control methods are not available. In the region of the curve (fig. 1) corresponding to grit size $\geq$1.0 μm, the "polishing" time corresponds to several hours of surface abrasion in order to ensure the maximum damage with each particular grit size. The polishing procedures used to obtain a given level of damage are difficult to describe because of the many variables and unknown factors involved. The goal was to prepare sapphire substrates with various levels of polishing damage, ranging from the best to the worst, as determined by infrared reflectance measurements.

Two approaches to polishing were used, as indicated above. In the first approach, substrates were purchased with ground surfaces, then lapped with 32-μm boron carbide grit, and "polished" with 15-μm diamond grit. Substrates were then sequentially polished with diamond grit of decreasing size (9 μm, 3 μm, 1 μm, 0.5 μm, 0.25 μm) on a bakelite surface ending with the grit size corresponding to the level of damage desired. A separate bakelite base was used for each grit size to avoid mixing particle sizes. Some substrates were polished with alumina on a Pellon* pad. The outer edges of some samples were polished with silica sol to provide a good surface finish at the periphery of the samples, while leaving about 0.5-in. diameter central region with the original diamond or alumina polish. In this manner two different surfaces were generated on the same substrate for ease of comparison of polishing effects in subsequent analysis. For example, x-ray topographs are more easily compared if the different surfaces being examined are present on the same sample. The same applied to the electrical characterization of heteroepitaxial silicon films. The best surfaces were prepared by polishing with silica sol, or were purchased from outside sources.

In the second approach, all substrates were highly polished initially and subsequently abraded with diamond grit of the desired particle size to give a range of damage as shown in figure 1.

Several sets of substrates, with a wide range of surface damage in each set, were prepared (and measured) for device application. Silicon films, 0.4 μm and 0.6 μm in thickness, were deposited on both annealed and unannealed sets of substrates. Silicon was deposited simultaneously on all members of a given set, and ultraviolet reflectance data (representing silicon film quality) were obtained at five positions on each wafer (four positions on the periphery, and one at the center on each wafer). The pattern described in reference [5] was then used in device fabrication and testing. All device testing was performed automatically and included: (1) gate threshold voltage, (2) device leakage current, (3) device drive current, and (4) drain breakdown voltage.

3. RESULTS AND DISCUSSION

3.1 Infrared Surface Characterization of Sapphire Substrates

Much of the technical data obtained in the characterization of sapphire substrates is discussed in references [8-10]. The following discussion will present additional data obtained later in the program. The specular reflectance spectra of variously polished ($1\bar{1}02$) sapphire surfaces for p and s polarizations are given in the references [8-10] together with

*See disclaimer, p. iii

the calculated optical constants for p polarization. The calculated optical constants for $(1\bar{1}02)$ sapphire using s polarization are presented in Table 1. As in the case of p polarization, the optical constants are strongly influenced by polishing damage. A discussion of the errors involved in the computed values of the optical constants is presented in reference [10].

Table 1. Calculated Optical Constants For $(1\bar{1}02)$ Sapphire, S Polarization, With Various Surface Polishes

Surface Finish	eV	λ, μm	σ, cm^{-1}	n	k
Standard	0.05158	24.0	416	44.4	
	0.05183	23.9	417.9		28.9
	0.06026	20.6	486	4.5	
	0.06051	20.5	488		5.2
	0.07192	17.2	580	29.3	
	0.07217	17.18	582		21.8
Linde A	0.05307	23.4	428	13.5	
	0.05332	23.3	430		8.2
	0.06026	20.6	486	1.98	
	0.06101	20.3	492		3.4
	0.07490	16.6	604	12.9	
	0.07614	16.3	614		10.4
1-μm Diamond	0.05258	23.6	424	6.4	
	0.05282	23.5	426		4.7
	0.06002	20.7	484	1.24	
	0.06076	20.4	490		2.3
	0.06721	18.5	542	2.25	
	0.06894	17.9	556		1.74
	0.07886	15.7	636	15.3	
	0.08010	15.5	646		9.1

3.2 Ultraviolet Surface Characterization of Heteroepitaxial Silicon Films On Sapphire

The technical basis for the characterization of silicon films by UV reflectance is discussed in reference [17]. Further discussion of the measurements will be presented later in this section.

3.3 Preliminary Correlations of Reflectance Data with Data from Other Measurements

An example of the correlation of infrared and ultraviolet reflectance data obtained on a set of variously polished sapphire substrates and corresponding heteroepitaxial silicon films, respectively, is shown in figure 2. The infrared reflectance ratios correspond to 10 reflections across each 1.5-in. diameter wafer. The ultraviolet reflectance measurements were made at two wavelengths, namely 2400 Å and 2800 Å on a relatively small area at the center of each silicon film. The data indicate that there is a good correlation between substrate surface quality and silicon film quality as determined optically. The silicon films were also analyzed by x-ray diffraction. Figure 3 shows a plot of diffraction peak half-width [θ : 2 θ scan, (400) diffraction plane] for the various silicon films vs the infrared reflectance ratio for the corresponding substrates. The larger the value of the diffraction peak half-width, the poorer the film quality. There also appears to be a good correlation between film quality, as determined by x-ray means, and initial substrate character. The shape of the curve in figure 3 is very similar to the shape of the curves in figure 2, indicating a correlation between ultraviolet reflectance and x-ray. This is shown in figure 4. Correlation of substrate reflectance data with x-ray linewidth broadening for damaged sapphire substrates has not been successful except for very high levels of damage. This is not surprising since the sampling depth in x-ray diffraction corresponds to

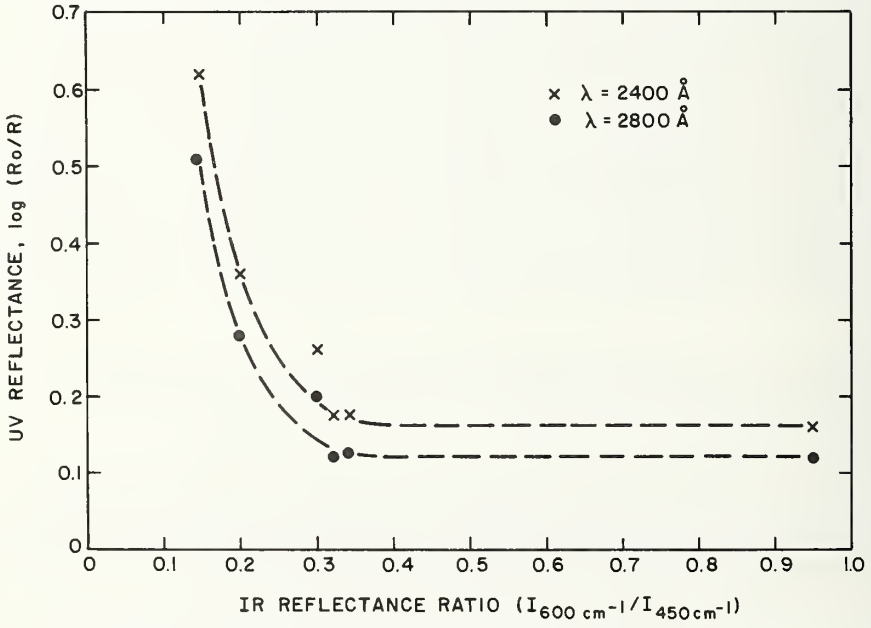

Figure 2. Correlation of infrared and ultraviolet reflectance data for sapphire and corresponding silicon-on-sapphire composites.

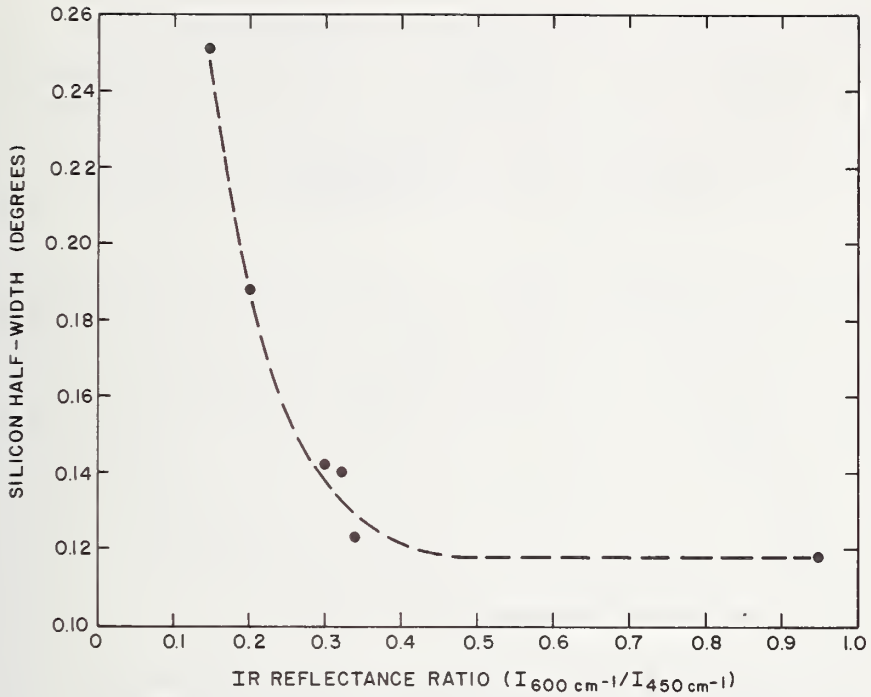

Figure 3. Correlation of x-ray diffraction peak half-width for various silicon films, with reflectance ratio for the corresponding sapphire substrates.

a penetration depth of several mil into the substrate surface, and the sensitivity of the method depends upon the fraction of the sampled volume which is damaged. By contrast, the infrared reflectance method corresponds to a penetration of less than 1000 Å. Thus, a correlation between the two methods would not be expected for relatively low levels of polishing damage.

The set of SOS composites, with various degrees of substrate surface damage, were subsequently ion-implanted and fabricated into device structures using the test pattern referred to previously. Electrical measurements were performed on n- and p-channel transistors and on gated-Hall bar devices on each wafer. Drain current corresponding to a given set of bias conditions on both transistor types is plotted vs infrared reflectance ratio for each substrate in figure 5. The bias conditions were the same in all cases, i.e., drain voltage was 5 V, and the gate voltage was 10 V, with appropriate polarity applied for both transistor types. Each data point, corresponding to drain current in figure 5, represents the average performance of about 120 devices across a diameter of a given wafer. It should be noted that in the preparation of sapphire surfaces the level of damage can vary across a surface. Usually, the level of damage is greatest toward the edges

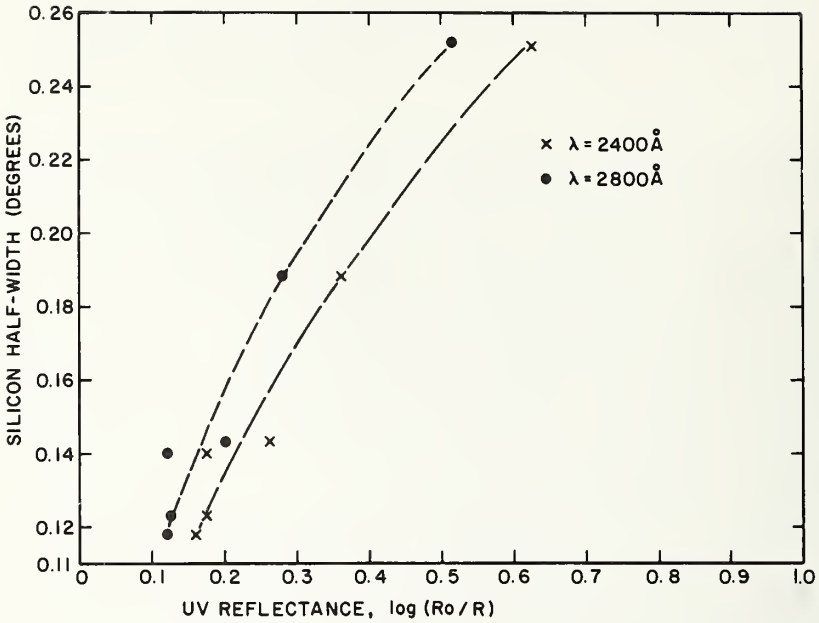

Figure 4. Correlation of x-ray diffraction peak half-width with ultraviolet reflectance for heteroepitaxial silicon on sapphire.

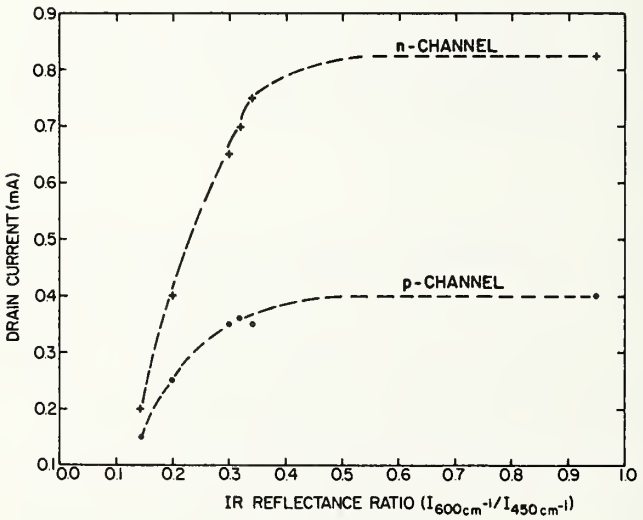

Figure 5. Correlation of SOS device channel current with infrared reflectance data for corresponding sapphire substrates.

of a wafer. Device performance across a given wafer may, thus, vary in a similar manner to the level of substrate surface damage. In the infrared multiple reflectance measurement, only a "figure of merit" for the surface quality of each substrate is obtained. For this reason, average device performance across a diameter of each wafer is plotted vs substrate infrared reflectance ratio in figure 5.

It is interesting to note (see fig. 5) that there appears to be little, if any, increase in drain current at a reflectance ratio above 0.5, although more data points are needed in this region on both curves to fully confirm this conclusion. These results suggest that there is a range of substrate surface damage which has very little influence on device performance in this experiment. It was determined that the threshold voltage was approximately the same for devices on all wafers except for the samples with the lowest infrared reflectance ratio (the most damaged substrates). Thus, the drain current is directly proportional to the field-effect mobility for those devices with the same threshold voltage. This indicates that field-effect mobility is also independent of the same range of damage as drain current, and threshold voltage is little affected by a relatively wide range of substrate surface damage. Gated-Hall mobility data for the same set of samples is plotted vs substrate infrared reflectance ratio in figure 6. The data

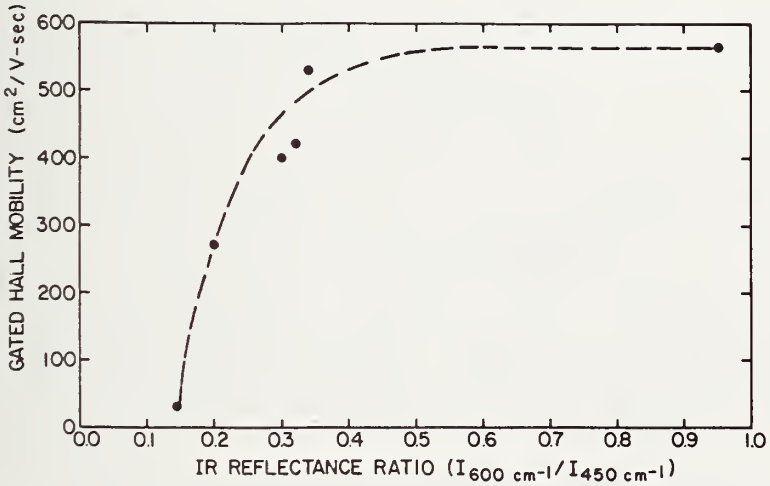

Figure 6. Correlation of gated-Hall mobility of SOS structures with infrared reflectance data of corresponding sapphire substrates.

in this figure are approximate because of the difficulty in making such measurements. Nevertheless, a similar trend is observed in this case also. The trends shown in figures 5 and 6 may be anticipated from the data presented in figure 2, provided the ultraviolet reflectance term

can be correlated with device performance. This correlation is shown in figures 7 and 8, which represent transistor current and Hall-mobility data from figures 5 and 6, respectively. (Note that the lower the ultraviolet reflectance term is, the better the silicon film quality.) No saturation trend is observed in these curves and improved device performance, as determined by the parameters measured here, can be expected from improved film crystallinity. However, it appears from figures 5 and 6 that substrate surface finishing is not the ultimate limiting factor in determining film quality.

Some comments regarding the data presented here are necessary. The infrared reflectance range shown in figures 5 and 6 corresponds approximately to the range observed (from the worst to the best) among purchased substrates.* The substrates used here were deliberately not annealed before silicon heteroepitaxy, except for one which had a good surface initially represented by a reflectance ratio of 0.95.

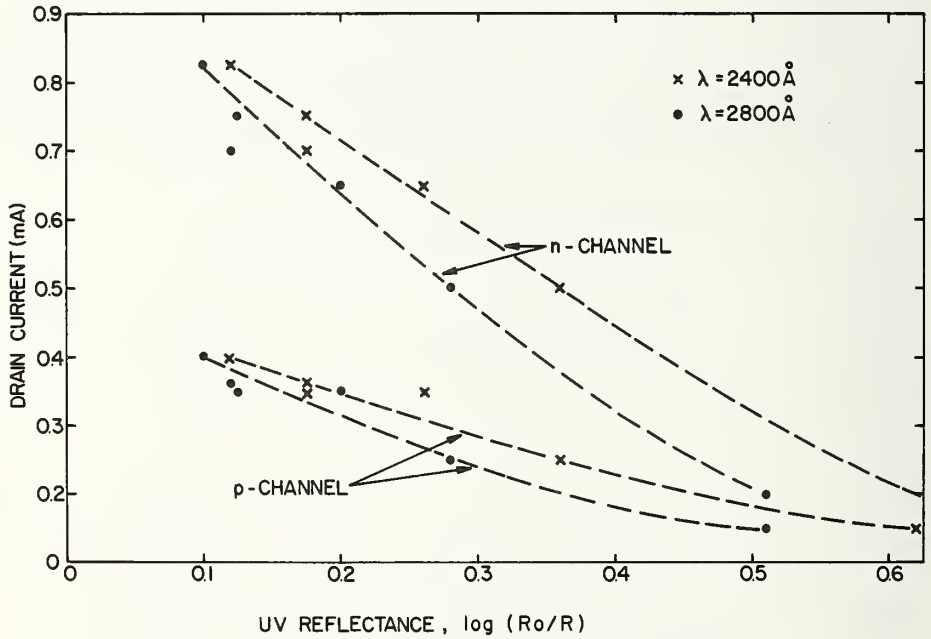

Figure 7. Correlation of SOS device channel current with ultraviolet reflectance data for corresponding epitaxial silicon films.

*Since this work was begun, there has been a considerable improvement in the surface quality of polished sapphire substrates. However, the possibility of proprietary annealing procedures could obscure the results of infrared analysis.

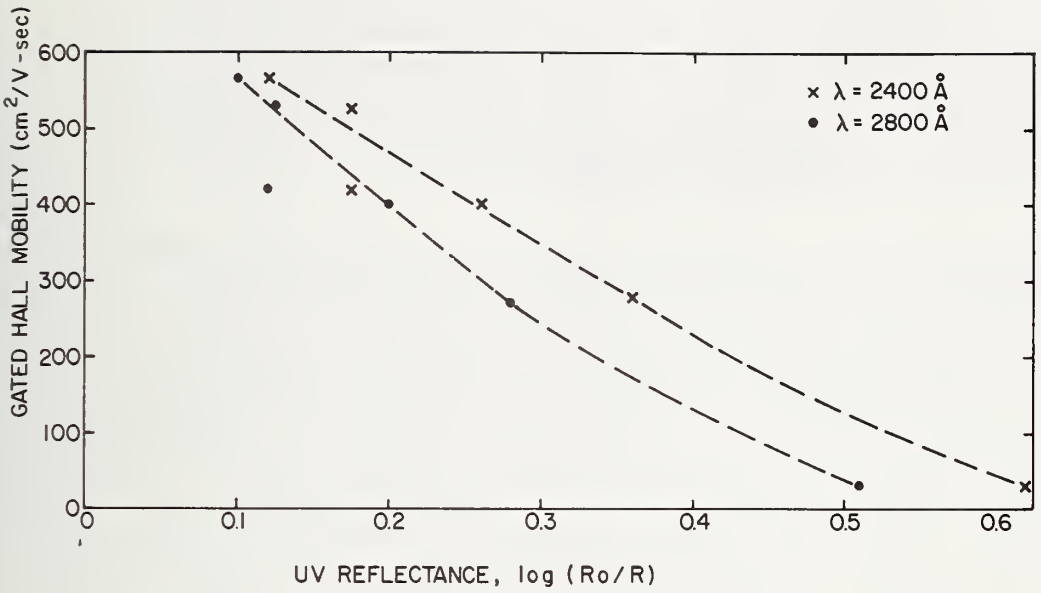

Figure 8. Correlation of gated-Hall mobility of SOS structures with ultraviolet reflectance data of corresponding epitaxial silicon films.

The latter served as a reference with which to rate the other samples in the experiment. Annealing the other substrates can be expected to improve device performance, but would obscure a decision on the level of damage tolerable in the substrate polishing process. The level of damage in the substrates used was not always uniform across the substrate. Consequently, some scatter in the data can be expected. In addition, gated-Hall measurements at the silicon film thickness used here (0.6 μm) are complex because of anomalous behavior near zero gate bias [22,23] and data must be obtained at a bias level suitable for the sample being evaluated. This means that all the measurements were not made under the same gate-bias conditions. Despite these factors, there is good correlation between the infrared reflectance measurements on the substrates, the ultraviolet reflectance measurements on the heteroepitaxial silicon films, and the electrical properties of the final devices.

3.4 Correlations of Device Data with Infrared Reflectance

These experiments were repeated with substrates having a similar range of damage as before but with more data points than shown in figure 5. All substrates used in this evaluation were highly polished initially and were selected so that the degree of substrate misorientation within a given set was similar. This was done to avoid effects of

substrate misorientation on field effect mobility [24]. Several sets of substrates were then abrasively polished with diamond grit to introduce the desired level of damage as shown in figure 1. Some substrate sets were annealed prior to silicon deposition, while others were used without annealing. Infrared reflectance measurements were made on all substrates prior to any annealing process.

Silicon films, 0.4 and 0.6 μm thick were deposited on both annealed and unannealed sets of substrates. Ultraviolet reflectance data (representing silicon film quality) are plotted vs the infrared reflectance data (representing the corresponding substrate surface quality) in figures 9 and 10 for 0.6- and 0.4-μm film thicknesses, respectively. A range is given for the variation in the ultraviolet reflectance term measured at five positions on each wafer (four positions on the periphery, and one at the center on each wafer). It can be seen from the data in figures 9 and 10 that annealing of highly damaged sapphire substrates greatly improves the quality of heteroepitaxial silicon films deposited on the substrates. The variation in silicon film quality, on a given damaged and subsequently annealed substrate, is also much reduced in comparison to the variation observed in film quality on the corresponding unannealed substrate. Thus, the dependence of silicon film quality on initial substrate surface damage is greatly diminished by substrate annealing prior to silicon deposition. However, for substrates characterized by infrared reflectance ratios greater than about 0.35, there appears to be a relatively small dependence of film quality on substrate polishing or annealing for both 0.4- and 0.6-μm thick silicon films. Referring back to figures 5 and 6, there appears to be a correlation between optical reflectance data from this set of experiments and previous experiments which were not organized in the same manner. This is important in deciding the viability of the optical reflectance methods in determining sapphire substrate quality and heteroepitaxial silicon film quality in relation to SOS device performance. The data indicate that the infrared reflectance technique is more sensitive to sapphire surface polishing than the electrical properties of silicon films deposited on the same substrates.

The second experimental set of SOS composites was fabricated into device structures using the same test pattern as before [5]. The silicon films were not ion-implanted in the channel region in this case so that device properties would be more characteristic of the materials used, i.e., not influenced by intentionally added dopant. Device properties across a diameter of each wafer corresponding to about 180 devices were automatically recorded. The basic tests were performed on n- and p-channel transistors (channel length = 7.62 μm, channel width = 15.2 μm). Statistical data were computed for each

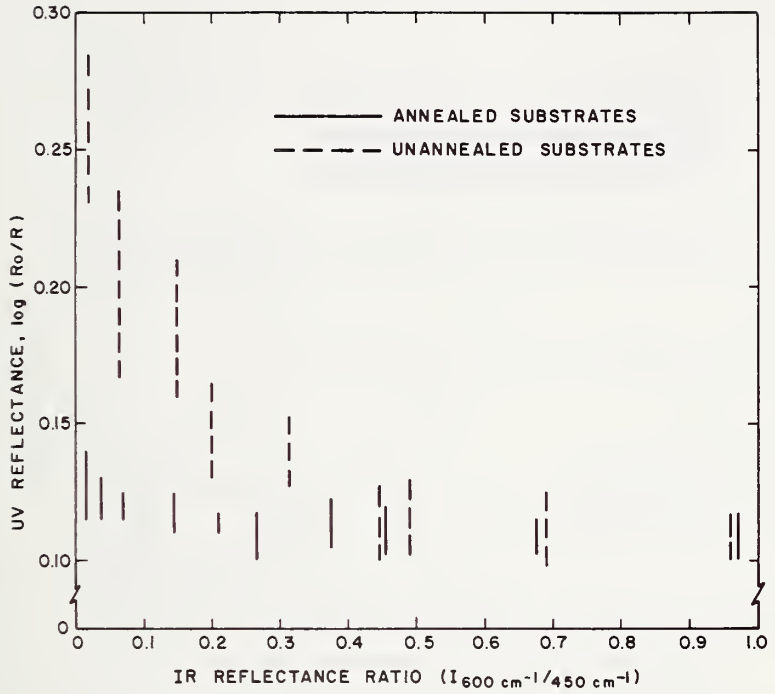

Figure 9. Plot of ultraviolet reflectance data (representing silicon film quality) vs infrared reflectance data (representing sapphire substrate surface quality). Silicon film thickness was 0.6 μm on all substrates.

parameter measured on the devices in a given scan across a wafer. In the following discussion mean values for the various device parameters are plotted vs initial substrate surface quality and silicon film quality as determined by optical reflectance. Data are provided for n- and p-channel devices on both annealed and unannealed substrates and for 0.6- and 0.4-μm-thick films.

Drain current for both n- and p-channel devices on both annealed and unannealed substrates is plotted vs initial substrate surface quality (IR reflectance ratio) in figures 11 and 12. These figures correspond to 0.6-μm and 0.4-μm silicon thickness, respectively. The biasing conditions were: drain voltage = 5 V, gate voltage = $|V_T| + 4$ V, with appropriate polarity applied for both transistor types. V_T is the extrapolated threshold voltage.

Important trends are observed in figures 11 and 12. The data obtained on unannealed substrates show no dependence on initial substrate surface quality above an infrared reflectance ratio of about 0.35. The

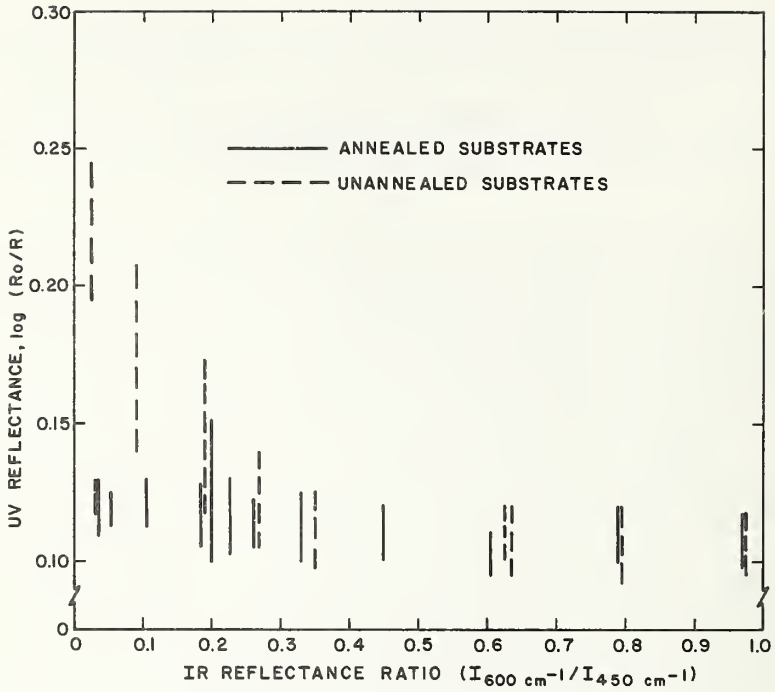

Figure 10. Plot of ultraviolet reflectance data (representing silicon film quality) vs infrared reflectance data (representing sapphire substrate surface quality). Silicon film thickness was 0.4 μm on all substrates.

drain current is independent of initial substrate surface quality (in the range studied) when substrates are annealed prior to silicon heteroepitaxial and device fabrication. Substrate annealing results in increased drain current even in the case of highly polished substrates. The trends observed in drain current also apply to field-effect mobility.

It is of interest to compare the data of figures 11 and 12 with those of figure 5. There appears to be a discrepancy in the values of the infrared reflectance ratio at which drain current reaches its final value. This can be explained as follows. The data in figure 5 were obtained on devices fabricated on 1.5-in. diameter sapphire substrates, while the data of figures 11 and 12 were obtained on 2.25-in. diameter substrates. In evaluating initial substrate surface quality, by infrared multiple reflectance measurements, about 10 reflections were used in the case of 1.5-in. diameter substrates and about 15 reflections in the case of 2.25-in. diameter substrates. The same reflectance jig was used in the measurement of the different substrates and the number of reflections

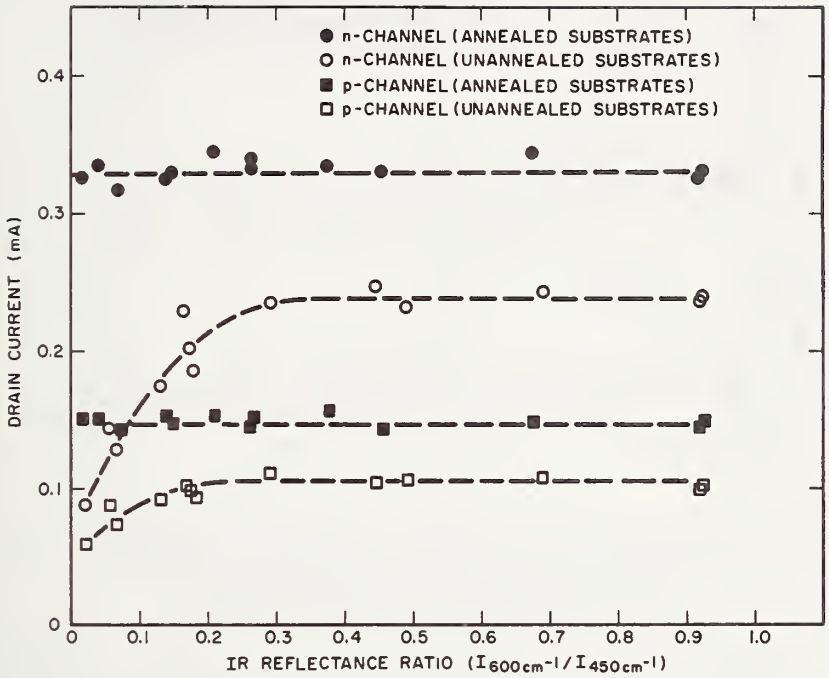

Figure 11. Plot of drain current, I_D, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.6 μm.

is limited by the wafer diameter. The measured multiple reflectance ratio for a given surface level of damage depends upon the number of reflections. Thus, it is necessary to show corresponding values of the reflectance ratio for 10 and 15 reflections on a given surface. Figure 13 shows this correspondence based on calculated data. For example, an infrared multiple reflectance ratio of 0.5 obtained with 10 reflections on a given sapphire surface corresponds to a reflectance ratio of 0.35 obtained with 15 reflections. This allows a comparison of the data in figures 11 and 12 with those in figure 5. In the case of unannealed substrates, the drain current reaches its final value at a reflectance ratio of about 0.5 in figure 5, and reaches its final value at about 0.35 in figures 11 and 12. These reflectance values represent the same level of substrate surface damage. It is interesting to note that the same substrate dependence is displayed in the results of the first and second sets of experiments despite the fact that the materials preparation, device fabrication methods, and operating conditions were

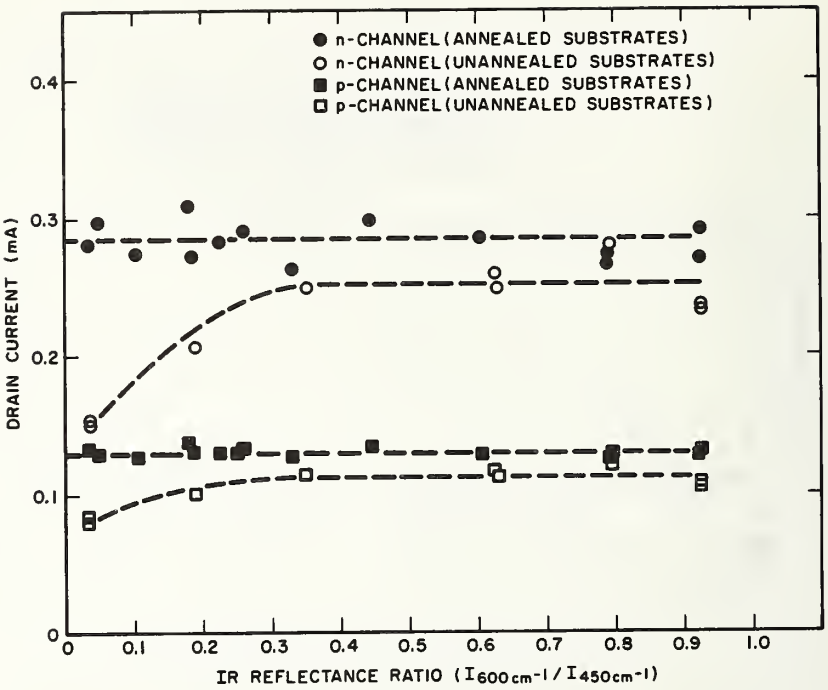

Figure 12. Plot of drain current, I_D, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.4 μm.

different in both experiments. These results are important in establishing the validity of the infrared reflectance technique as a reliable method of determining sapphire surface quality. The differences in drain current shown in figures 5 and 11 for silicon films, 0.6 μm thick, results from different doping levels, gate-bias conditions, and device fabrication methods. The enhancement of device field-effect mobility on annealed substrates, which initially had a wide range of surface damage, may be related to surface reconstruction and elimination of impurities [25]. Even the best polished surfaces show enhanced device field-effect mobility if annealed prior to silicon heteroepitaxy. The infrared reflectance method is not sensitive to this change. The effect of annealing may be due in part to a surface cleaning process. The resistivity of silicon films on annealed substrates is generally lower than that of films on unannealed substrates.

Figures 14 and 15 give the mean values of drain current vs substrate surface quality for the same set of devices (referred to in figures 11 and 12) when the biasing conditions were: drain voltage = 5 V and gate

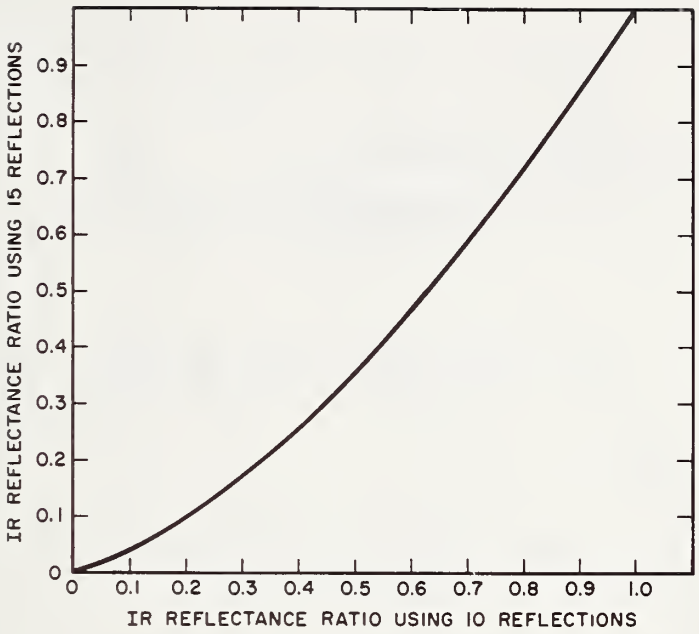

Figure 13. Dependence of infrared reflectance ratio on number of reflections for a range of sapphire surface damage.

voltage = 5 V, with appropriate polarity. In this case the drain current is influenced by field-effect mobility and threshold voltage changes. The trends observed in these figures are similar to those in figures 11 and 12, indicating the same basic dependence on substrate surface quality. An unexpected trend in the figures shows that the drain current for devices fabricated on unannealed substrates in 0.4-μm silicon films is higher than for 0.6-μm-thick films, indicating a higher carrier concentration. The ratio of the resistivities was, qualitatively, about 3:1 for 0.6-μm and 0.4-μm-thick films on unannealed substrates. The opposite trend occurred on annealed substrates except that there was relatively little difference in resistivity between the two film thicknesses.

The computed standard deviations, for the preceding data relating to drain current, are presented in figures 16 through 19. The principal trend is an increase in the standard deviation, σ, at low infrared reflectance ratios, particularly in the case of n-channel devices on unannealed substrates.

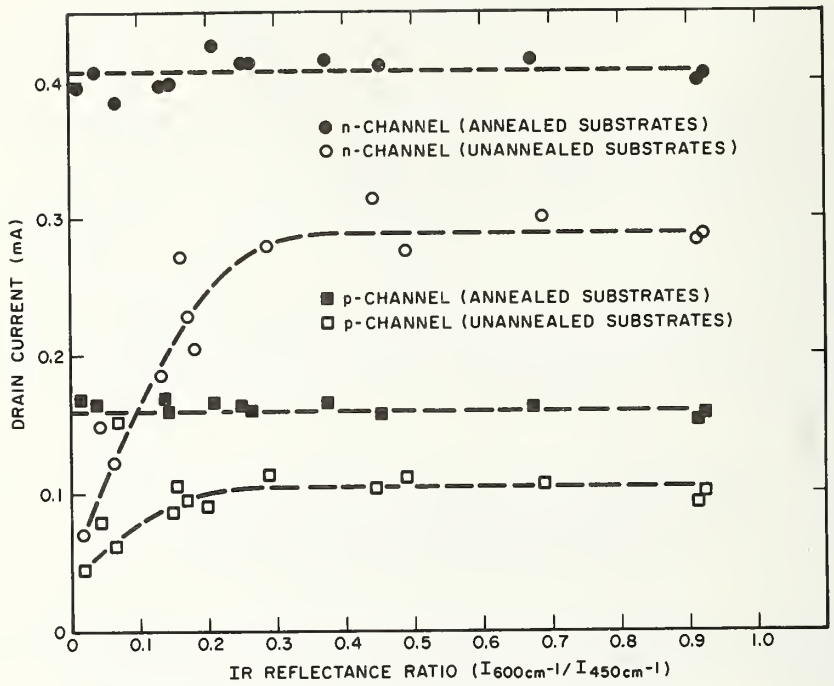

Figure 14. Plot of drain current, I_D, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 5$ V, silicon film thickness = 0.6 μm.

The electrical data presented in the foregoing discussion represent the mean values and standard deviations for approximately 180 devices across a wafer. Several factors can result in scatter in the data when the values are plotted vs initial substrate surface quality. As indicated, substrates are frequently curved giving rise to nonuniform damage across a given substrate and usually with an increasing level of damage at the edges. Thus, the multiple reflectance ratio for a given substrate is only an average quality factor for that surface. In addition, the reflectance may not have been measured across the same wafer diameter over which devices were subsequently measured. In device fabrication, wafer edge effects frequently cause abnormal device characteristics, and depending upon the frequency of such abnormal edge devices, the mean value of the parameter being measured can be affected by factors not related to substrate surface quality. Device parameters can also be influenced by device processing so that only a partial

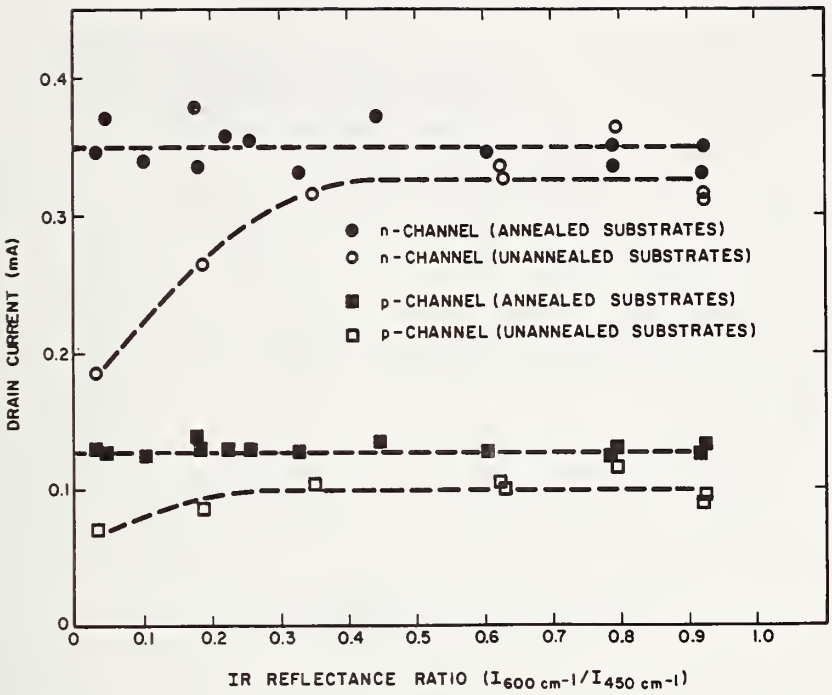

Figure 15. Plot of drain current, I_D, vs infrared reflectance ratio, $|V_D|$ = 5 V, $|V_G|$ = 5 V, silicon film thickness = 0.4 μm.

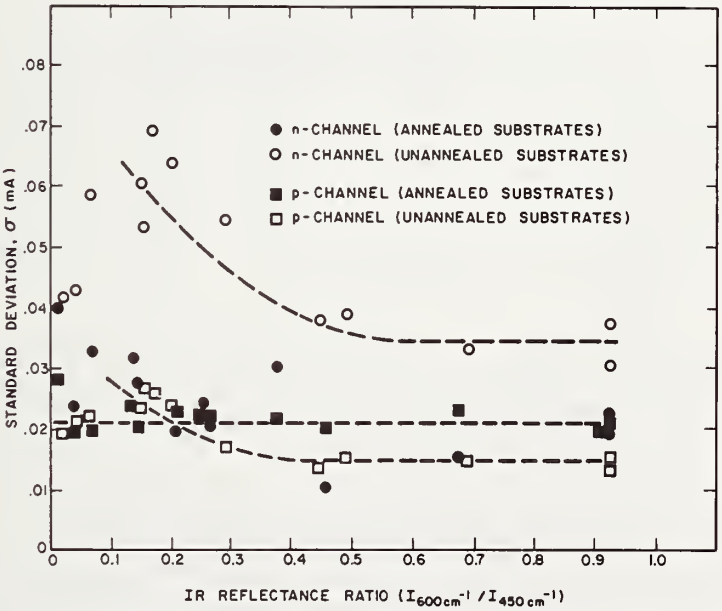

Figure 16. Plot of standard deviation for I_D vs infrared reflectance ratio, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = $|V_T|$ + 4 V, silicon film thickness = 0.6 μm (see fig. 11).

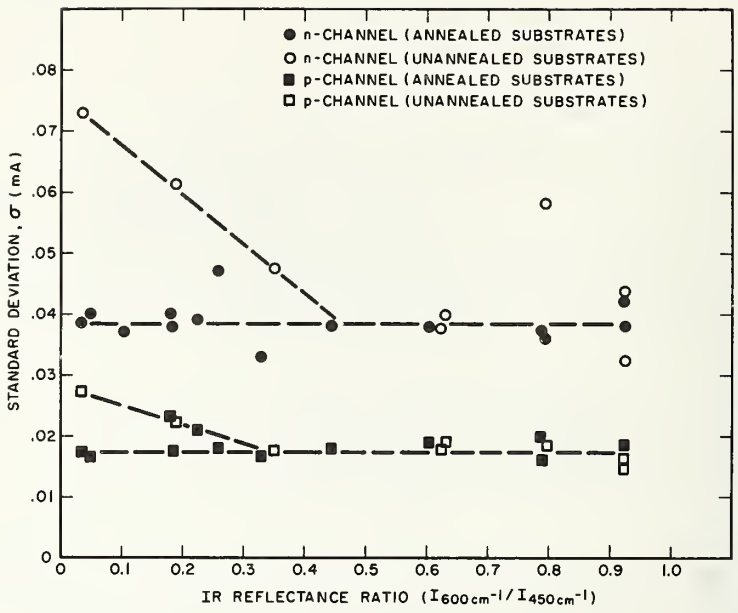

Figure 17. Plot of standard deviation for I_D vs infrared reflectance ratio, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = $|V_T|$ + 4 V, silicon film thickness = 0.4 μm (see fig. 12).

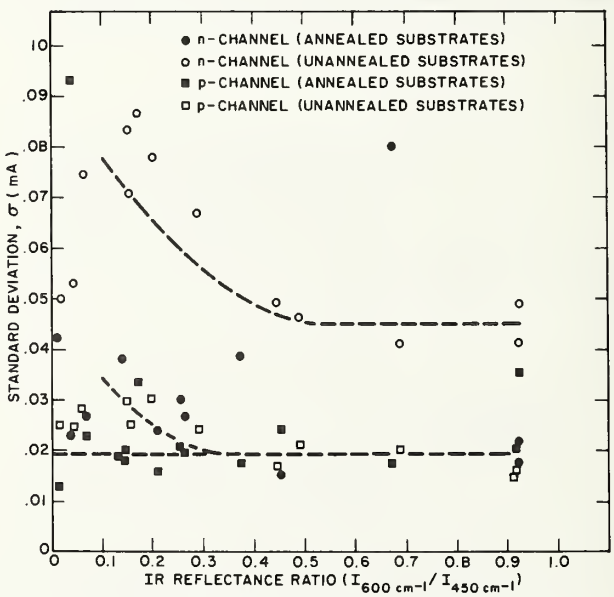

Figure 18. Plot of standard deviation for I_D vs infrared reflectance ratio, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = 5 V silicon film thickness = 0.6 μm (see fig. 14).

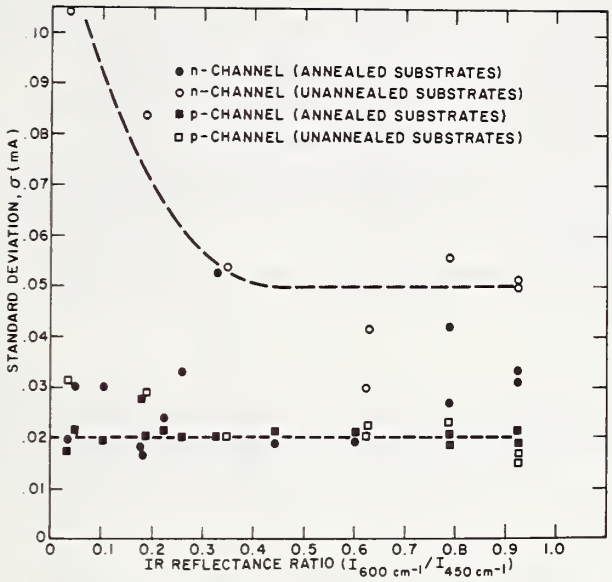

Figure 19. Plot of standard deviation for I_D vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 5$ V, silicon film thickness = 0.4 μm (see fig. 15).

correlation may exist with substrate quality. No attempt has been made to minimize these effects in the data of the previous figures. In order to understand the influence of the effects just described, it is necessary to examine the profile for each parameter measured across each wafer together with the statistical data for the parameter measured on each wafer. A complete description of the analysis is given in reference [5]. The standard deviations are subject to the same type of scatter as the mean values. These observations also apply to the following results.

The extrapolated threshold voltage values for n- and p-channel devices on both annealed and unannealed substrates are given in figures 20 and 21, which correspond to 0.6- and 0.4-μm-thick silicon films, respectively. Again, each data point in these figures represents the mean value for about 180 devices across each wafer and is plotted vs the infrared reflectance ratio for the corresponding substrate surface. As in the case of drain current, the extrapolated threshold voltage is independent of initial substrate surface quality above a reflectance ratio of about 0.35 in the case of unannealed substrates, and is completely independent of initial surface quality (over the range studied) in the case of annealed substrates. At ratios >0.35, the threshold

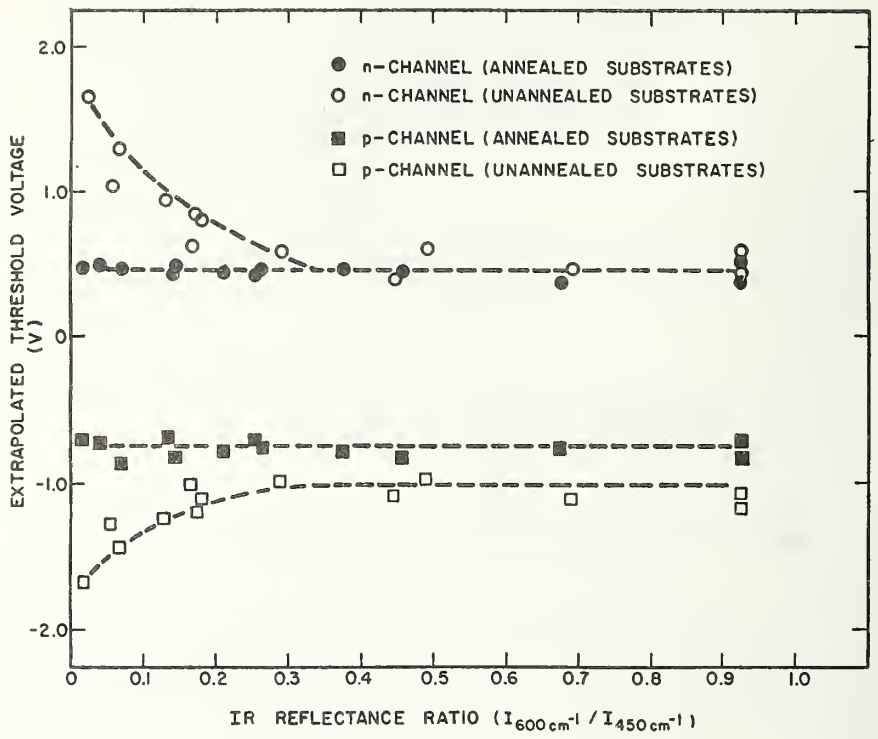

Figure 20. Plot of extrapolated threshold voltage, V_T, vs infrared reflectance ratio, silicon film thickness = 0.6 μm.

voltage of p-channel devices is higher on unannealed substrates than on annealed substrates while the threshold voltage of n-channel devices appears to be about the same on both substrate types. At reflectance ratios below 0.35, the threshold voltage of both n- and p-channel devices on unannealed substrates increases with decreasing reflectance ratios. This is probably due to the increasing defect structure of the films. In general, the threshold voltage of n-channel devices on both annealed and unannealed substrates is higher in the case of 0.6-μm-thick films than for 0.4-μm-thick films. The reverse situation occurs with p-channel devices.

The standard deviation for extrapolated threshold voltage, figures 22 and 23, is independent of substrate surface quality in the case of annealed substrates. It is generally higher in the case of unannealed substrates and increases at reflectance ratios below about 0.35. In addition, the standard deviation in the case of 0.4-μm-thick silicon

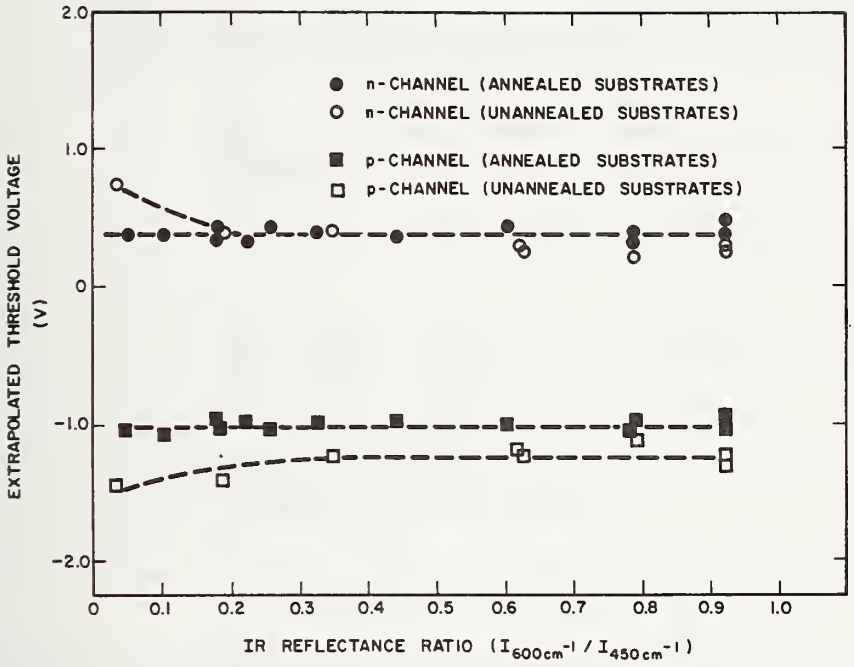

Figure 21. Plot of extrapolated threshold voltage, V_T, vs infrared reflectance ratio, silicon film thickness = 0.4 μm.

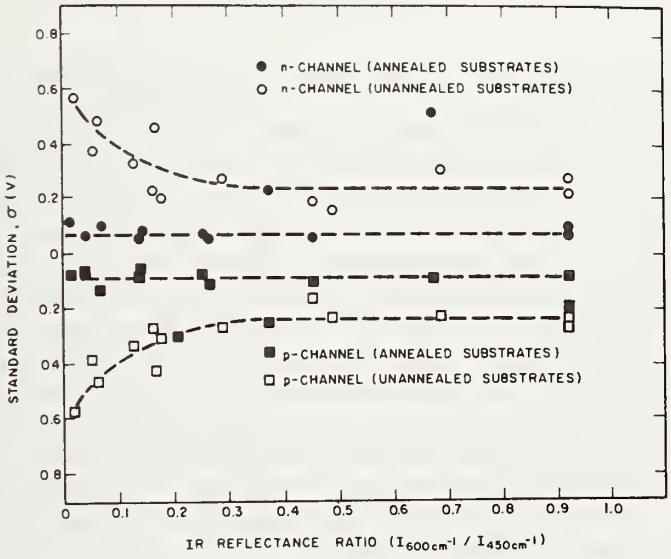

Figure 22. Plot of standard deviation for V_T vs infrared reflectance ratio, silicon film thickness = 0.6 μm (see fig. 20).

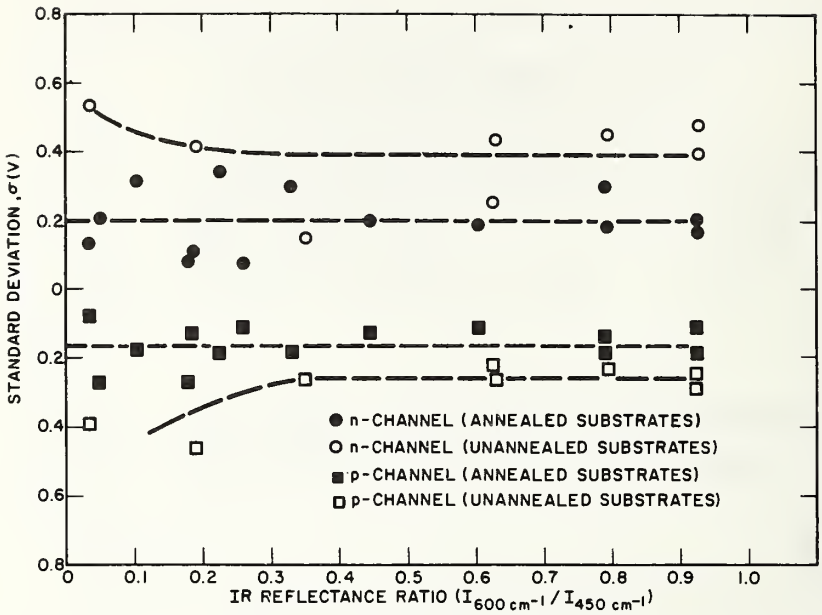

Figure 23. Plot of standard deviation for V_T vs infrared reflectance ratio, silicon film thickness = 0.4 μm (see fig. 21).

films tends to be higher than for 0.6-μm-thick films. The data in figures 22 and 23 are plotted in a similar manner to figures 20 and 21 for convenience.

Device leakage current was also included in the evaluation. There is considerable scatter in the results indicating that other factors besides substrate surface quality are involved in determining leakage current. The following discussion deals with the more obvious trends. Figures 24 and 25 give the computed mean values of leakage current when $|V_D| = 5$ V, and $|V_G| = 0$ V. In the case of annealed substrates there appears to be little correlation between leakage current and initial substrate surface quality. In the case of unannealed substrates there appears to be little dependence on substrate surface quality above a reflectance ratio of about 0.35. At lower reflectance ratios the leakage current of n-channel devices decreases and the leakage current of p-channel devices tends to increase slightly. The effect is more pronounced for n-channel devices and for 0.6-μm-thick films. Figures 26 and 27 give the corresponding computed mean values for leakage current when both n- and p-channel devices are biased in the "off" condition with 2 V of appropriate polarity on the gate of each device. There is relatively little change in the leakage current of p-channel devices as a result of changing the gate voltage from 0 V to 2 V. This

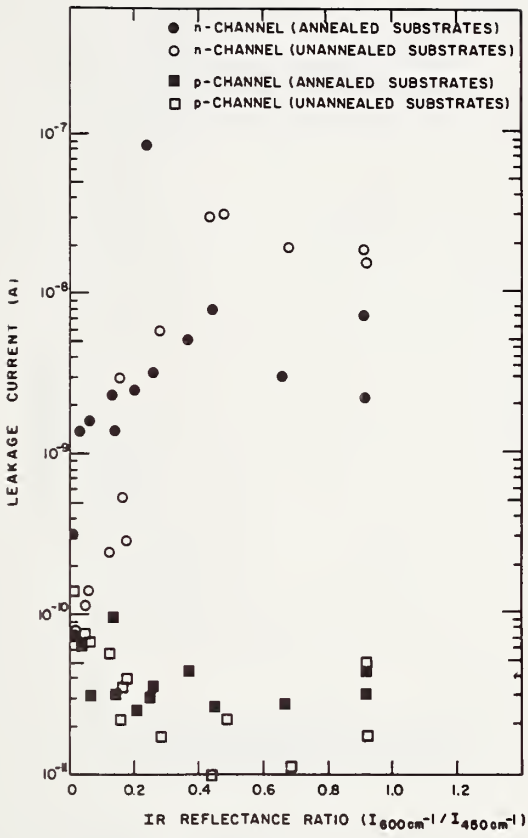

Figure 24. Plot of leakage current, I_L, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.6 μm.

applies to both annealed and unannealed substrates. By contrast, the leakage current of n-channel devices decreases by up to two orders of magnitude by changing the gate voltage from 0 V to -2 V for both annealed and unannealed substrates, irrespective of initial substrate surface quality. This simply reflects the presence of a low n-channel threshold voltage. As indicated previously, the silicon films were not ion-implanted in the channel region. The most significant aspect of these results is that substrate surface damage does not lead to higher leakage currents than is characteristic of SOS devices on highly polished sapphire substrates.

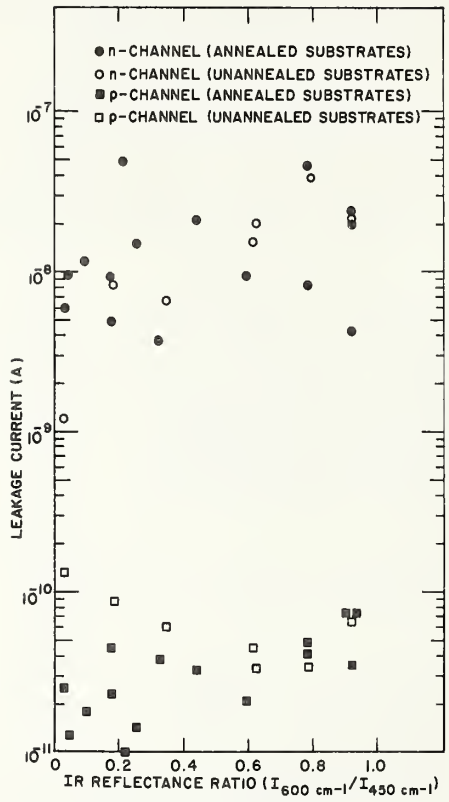

Figure 25. Plot of leakage current, I_L, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.4 μm.

The standard deviation, σ, for leakage current (figs. 28 through 31) shows similar trends, in relation to substrate quality, as were observed in the case of the mean values of leakage current. The value of σ for leakage current is usually larger than the mean value. The reason for this can be explained as follows: the distribution of device parameters across the diameter of a given wafer is usually relatively uniform except at the wafer edges. Localized exceptions to this observation can exist but are relatively few statistically. Edge device parameters have been included in the statistical analysis and can cause a substantial increase in magnitude of the standard deviation for a particular device parameter. This is particularly true in the case of leakage current. In the latter case, the threshold voltage values of devices at the periphery of each wafer may differ from the

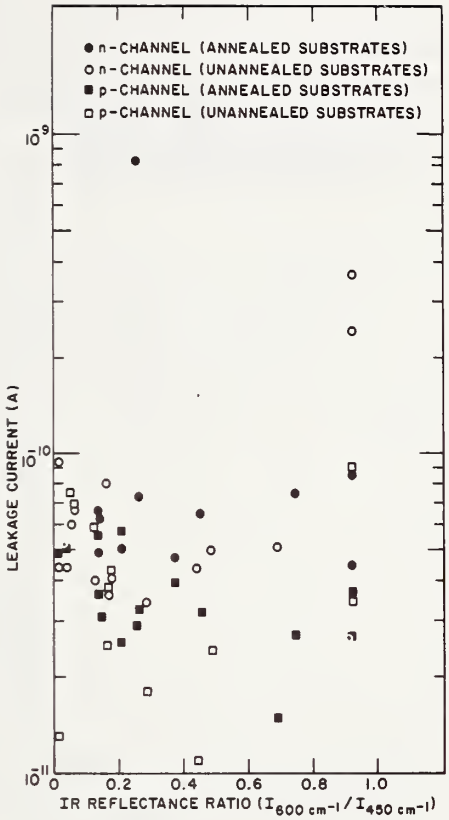

Figure 26. Plot of leakage current, I_L, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 2$ V in the "off" condition for both transistor types, silicon film thickness = 0.6 μm.

values for devices across most of the wafer, thus causing a difference in apparent leakage current of devices located at the wafer edges and those distributed across most of the wafer. For this reason, the standard deviation for leakage current (or other small quantity) can be strongly influenced by edge device effects. The magnitude of σ for leakage current would be much reduced if wafer edge devices were excluded from the statistical data. Consequently, the magnitude of σ for leakage current relative to the mean value of leakage current is of little significance in this presentation, and is used only for comparing device performance on variously polished substrates. The most important point, however, is that substrate surface damage does not

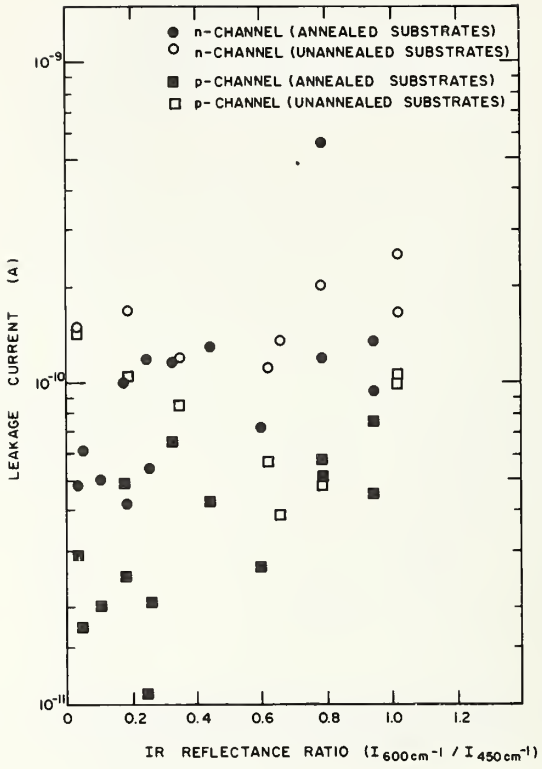

Figure 27. Plot of leakage current, I_L, vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 2$ V in the "off" condition for both transistor types, silicon film thickness = 0.4 μm.

result in an increase in the mean value or the standard deviation for leakage current. Evidently, other factors besides substrate surface damage are responsible for determining leakage current.

Figures 32 and 33 give the mean values of drain breakdown voltage, V_{BV} under "hard-off" conditions, i.e., $|V_G| = 2$ V. The breakdown voltage corresponds to the voltage required to force a drain current of 10 μA. The value of V_{BV} is essentially independent of initial substrate surface quality when substrates are annealed prior to epitaxy. There is little if any dependence of V_{BV} on substrate surface quality

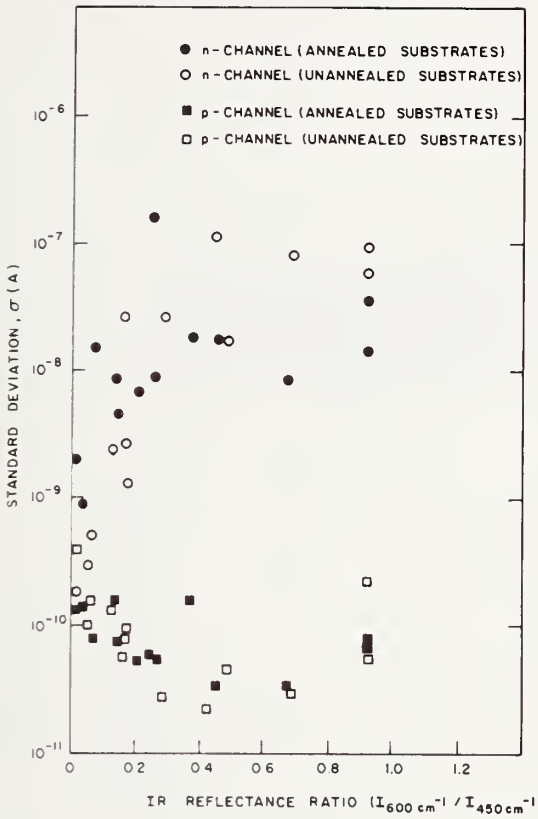

Figure 28. Plot of standard deviation for I_L vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.6 μm (see fig. 24).

in the case of n-channel devices on unannealed substrates, and the breakdown voltage of p-channel devices increases with increasing surface damage at reflectance ratios <0.35. There is no dependence in the latter case at reflectance ratios above 0.35. Substrate annealing results in lower drain breakdown voltages and the effect is more pronounced in the case of 0.6-μm-thick silicon films.

The standard deviation for drain breakdown voltage (figs. 34 and 35) shows little dependence on substrate quality except for the very worst substrates; p-channel devices on unannealed substrates appear to be influenced more than n-channel devices.

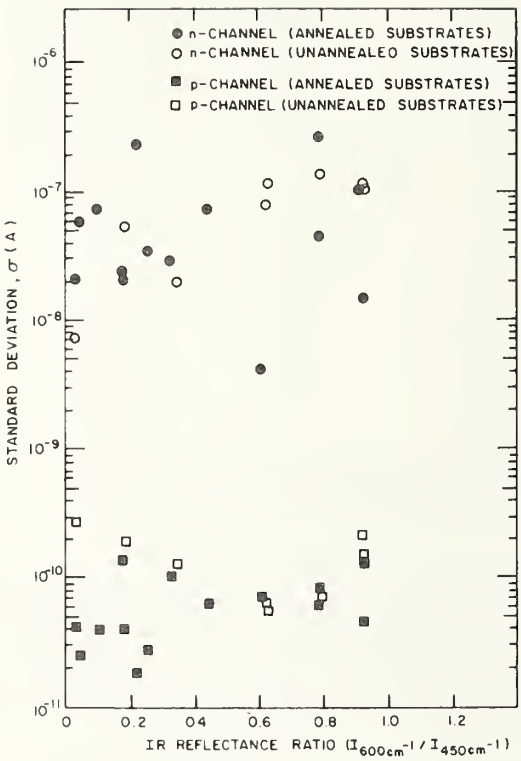

Figure 29. Plot of standard deviation for I_L vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.4 μm (see fig. 25).

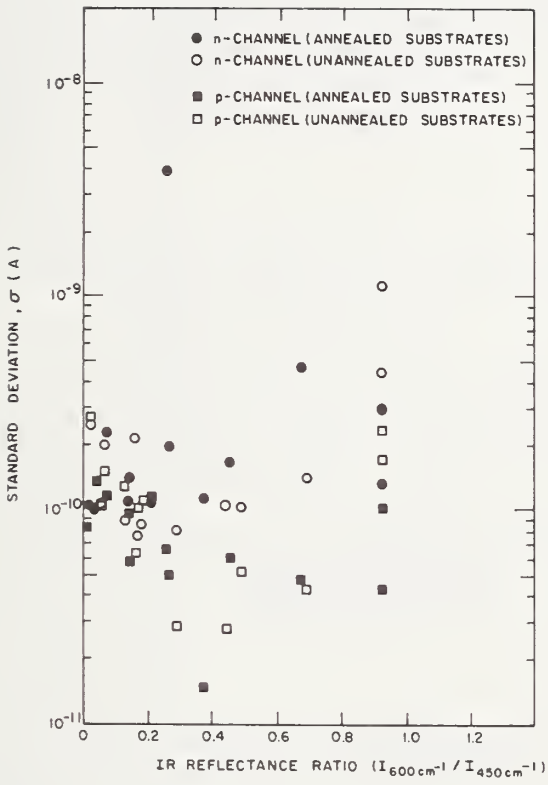

Figure 30. Plot of standard deviation for I_L vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 2$ V in the "off" condition for both transistor types, silicon film thickness = 0.6 μm (see fig. 26).

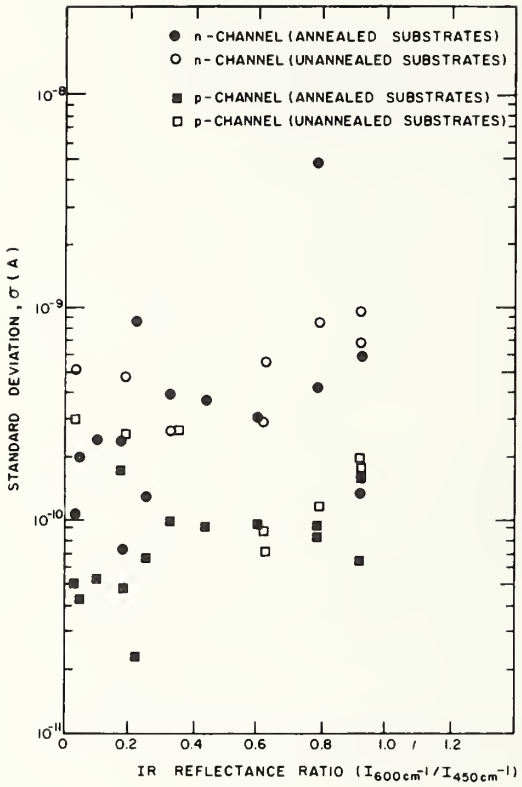

Figure 31. Plot of standard deviation for I_L vs infrared reflectance ratio, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 2$ V in the "off" condition for both transistor types, silicon film thickness = 0.4 μm (see fig. 27).

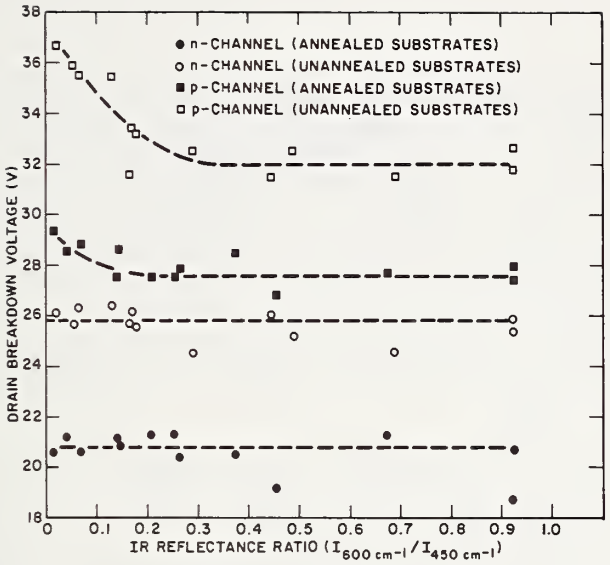

Figure 32. Plot of drain breakdown voltage, V_{BV}, vs infrared reflectance ratio, transistor biasing condition: $|V_G| = 2$ V in the "off" condition ($I_D = 10$ μA), silicon film thickness = 0.6 μm.

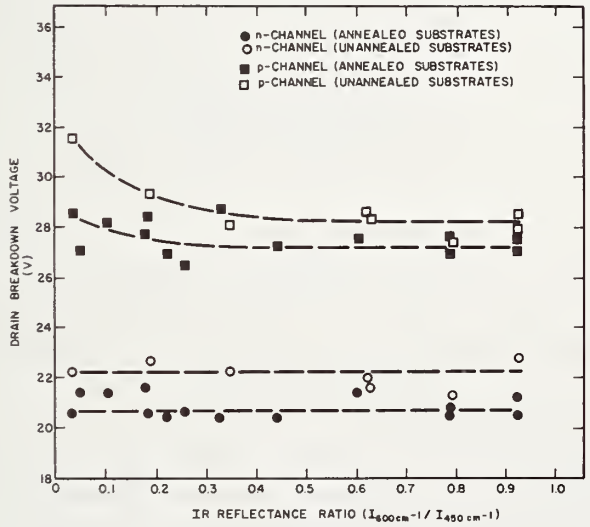

Figure 33. Plot of drain breakdown voltage, V_{BV}, vs infrared reflectance ratio, transistor biasing condition: $|V_G| = 2$ V in the "off" condition ($I_D = 10$ μA), silicon film thickness = 0.4 μm.

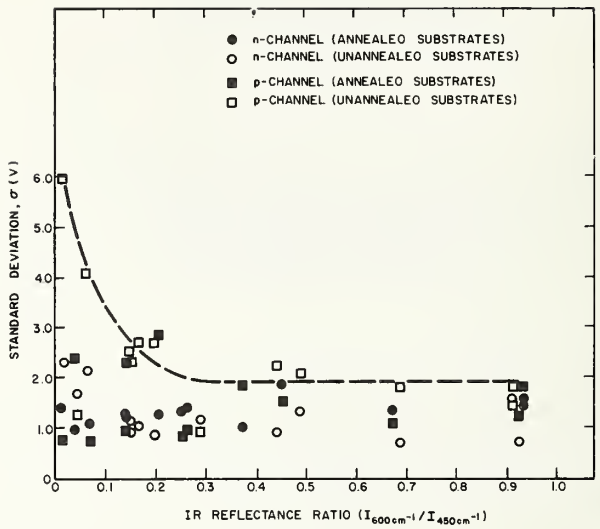

Figure 34. Plot of standard deviation for V_{BV} vs infrared reflectance ratio, transistor biasing condition: $|V_G|$ = 2 V in the "off" condition (I_D = 10 μA), silicon film thickness = 0.6 μm (see fig. 32).

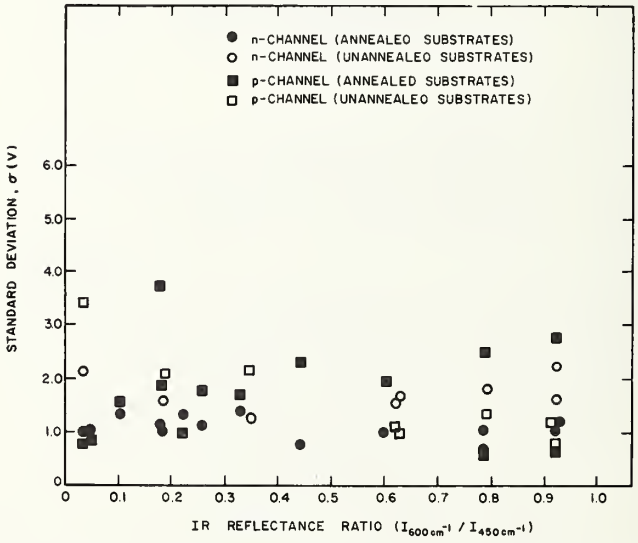

Figure 35. Plot of standard deviation for V_{BV} vs infrared reflectance ratio, transistor biasing condition: $|V_G|$ = 2 V in the "off" condition (I_D = 10 μA), silicon film thickness = 0.4 μm (see fig. 33).

3.5 Correlations of Device Data with Ultraviolet Reflectance

The following discussion deals with the trends observed in device parameters as a function of silicon film quality, which was determined by ultraviolet reflectance measurements. Film quality is expressed as the average value of the results of three ultraviolet measurements across the same wafer diameter as scanned in device measurement. The three ultraviolet measurements were made at the center and two opposite edges of the wafer diameter described. The average value of the ultraviolet reflectance parameter is plotted vs the corresponding infrared reflectance ratio for each substrate surface in figures 36 and 37. These figures represent 0.6- and 0.4-μm-thick films, respectively.

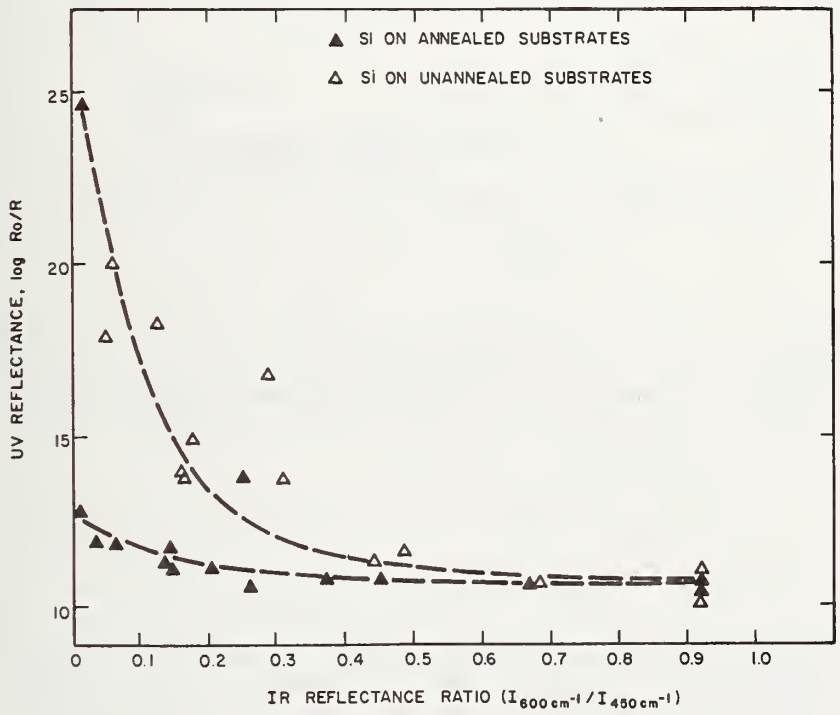

Figure 36. Correlation of the results of ultraviolet reflectance measurements on heteroepitaxial silicon films with the results of infrared reflectance measurements on the corresponding sapphire substrates, silicon film thickness = 0.6 μm.

In subsequent figures, the mean values of device parameters are plotted vs the average ultraviolet reflectance parameter. These

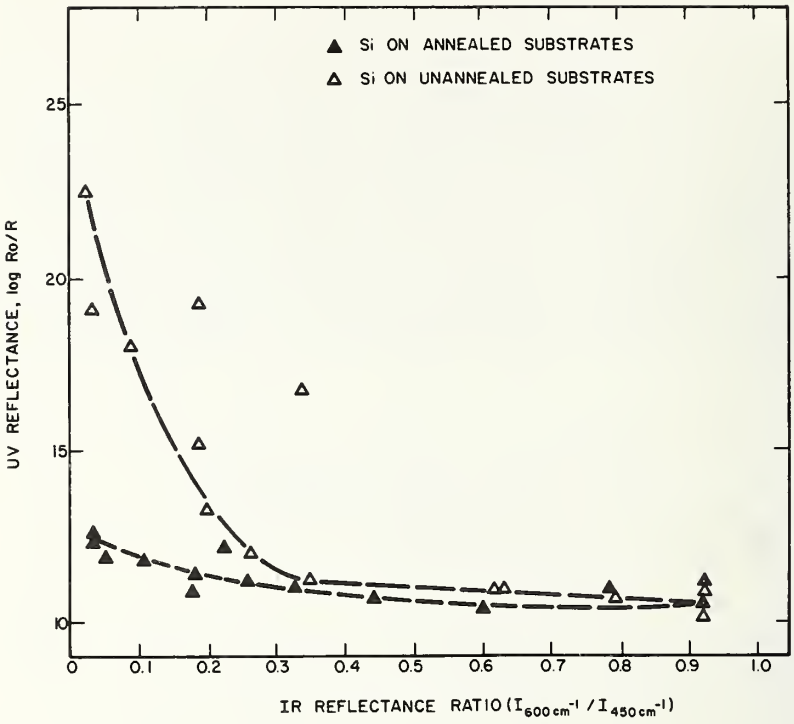

Figure 37. Correlation of the results of ultraviolet reflectance measurements on heteroepitaxial silicon films with the results of infrared reflectance measurements on the corresponding sapphire substrates, silicon film thickness = 0.4 μm.

figures should be studied in conjunction with figures 36 and 37, and the preceding figures relating device performance to substrate surface quality.

Figures 38 through 41 show drain current vs the ultraviolet reflectance term for the corresponding silicon films. The value of the ultraviolet reflectance term and the drain current for n- and p-channel devices cover a narrow range in the case of films on annealed substrates (irrespective of the initial level of substrate surface damage). In the case of devices on unannealed substrates, the drain current increases as the ultraviolet reflectance term decreases, i.e., as film quality improves. These trends would be expected from the previous discussion. It may also be noted that drain current for devices on

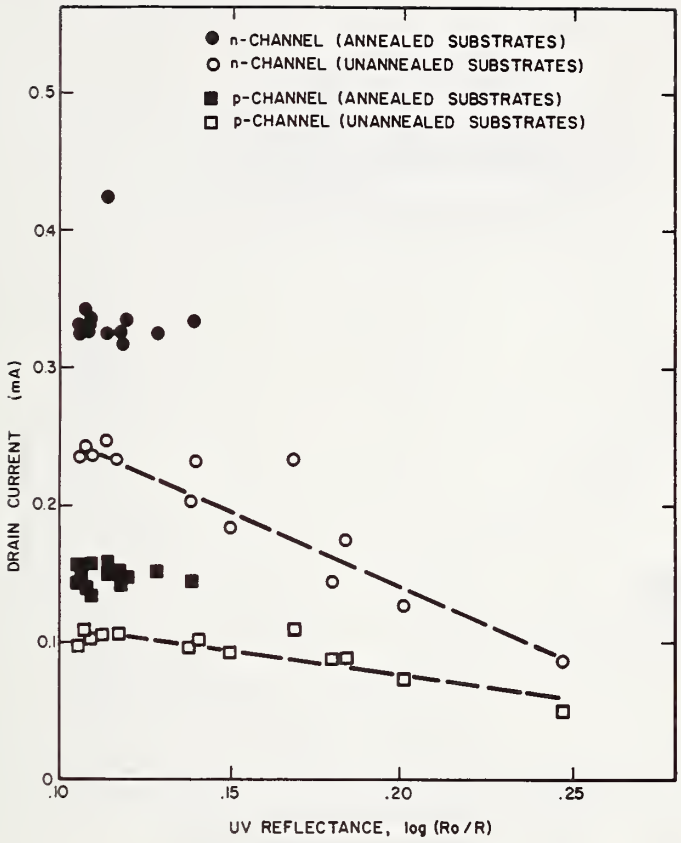

Figure 38. Plot of drain current, I_D, vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.6 μm.

both annealed and unannealed substrates does not converge to the same final value at low ultraviolet reflectance ratios. This result is consistent with previous results on the dependence of drain current on substrate surface quality (see e.g., figs. 11, 12, 14, and 15). These data indicate that, although the reflectance methods may indicate good substrate and silicon film quality, higher drain currents (and field-effect mobilities) are observed on annealed than on unannealed substrates. This is true even in the case of the best polished surfaces, and is more pronounced for 0.6-μm-thick film than for 0.4-μm-thick film. The data indicate that substrate annealing is more important than substrate polishing. The influence of annealing is not fully

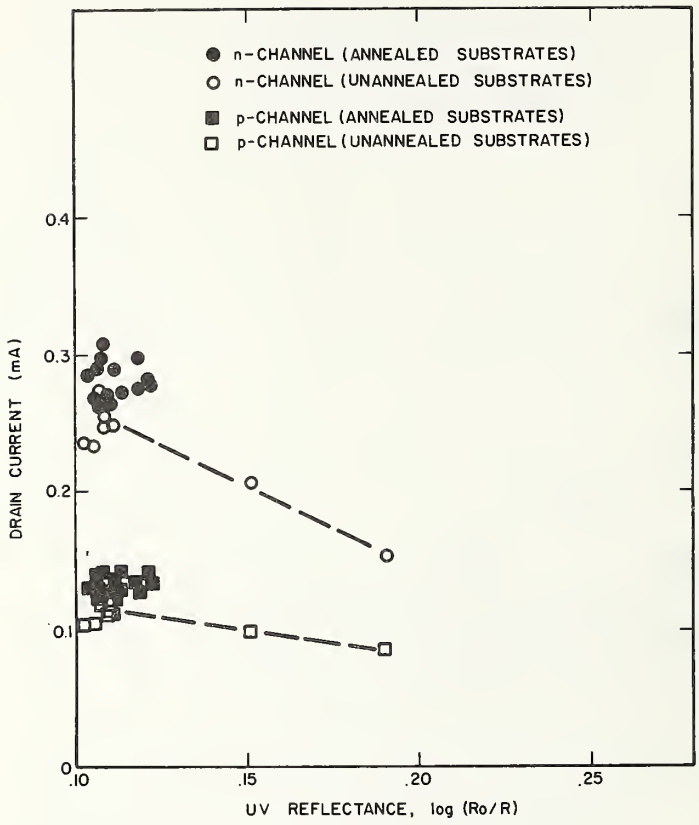

Figure 39. Plot of drain current, I_D vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.4 μm.

understood. In general, the resistivity of films on annealed substrates is lower than on unannealed substrates and the defect structure may also be lower. The beneficial effects of annealing are less evident when thinner films, e.g., 0.4 μm, are used, probably due to the increasing defect density of the films as the sapphire surface is approached [26]. In this case, the drain current for devices on both annealed and unannealed substrates tends to approach the same final value at low ultraviolet reflectance ratios.

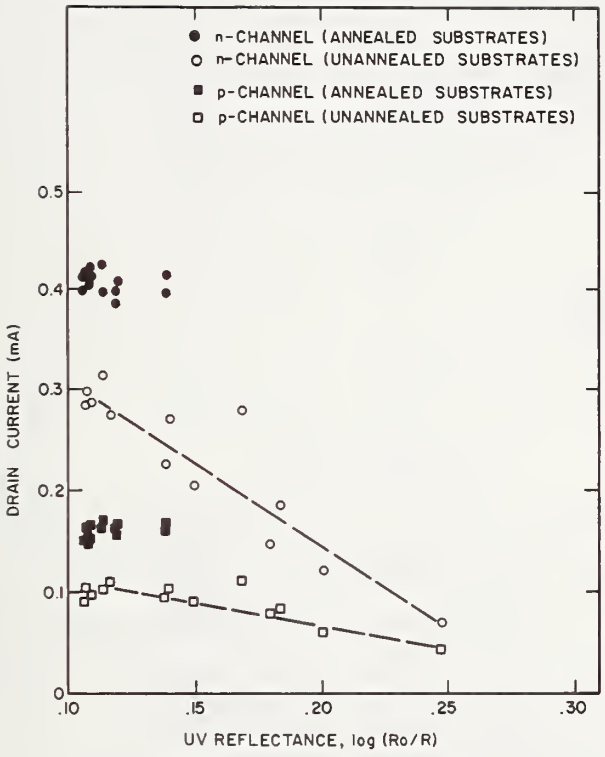

Figure 40. Plot of drain current, I_D, vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 5$ V, silicon film thickness = 0.6 μm.

The standard deviation for drain current as a function of ultraviolet reflectance is shown in figures 42 through 45. There is little dependence of σ on the ultraviolet reflectance term in the case of annealed substrates. In general, the value of σ increases as the ultraviolet reflectance term increases in the case of unannealed substrates, n-channel devices being more noticeably affected.

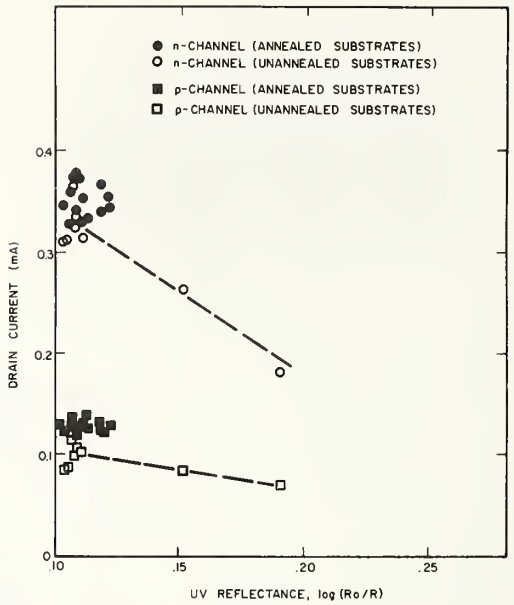

Figure 41. Plot of drain current, I_D, vs ultraviolet reflectance, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = 5 V, silicon film thickness = 0.4 μm.

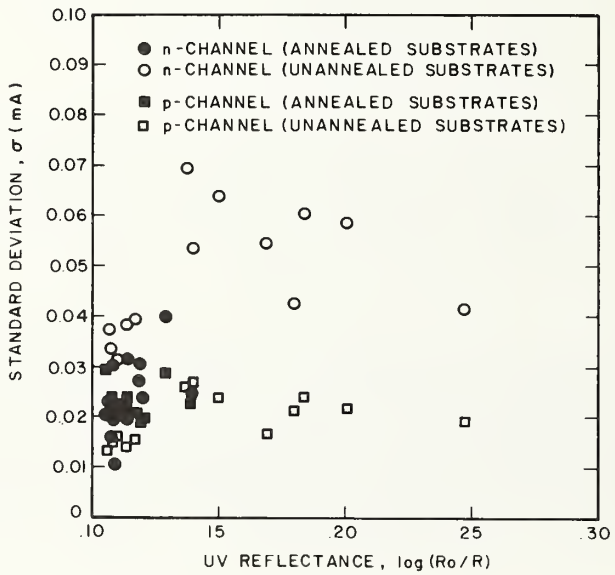

Figure 42. Plot of standard deviation for I_D vs ultraviolet reflectance, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.6 μm (see fig. 38).

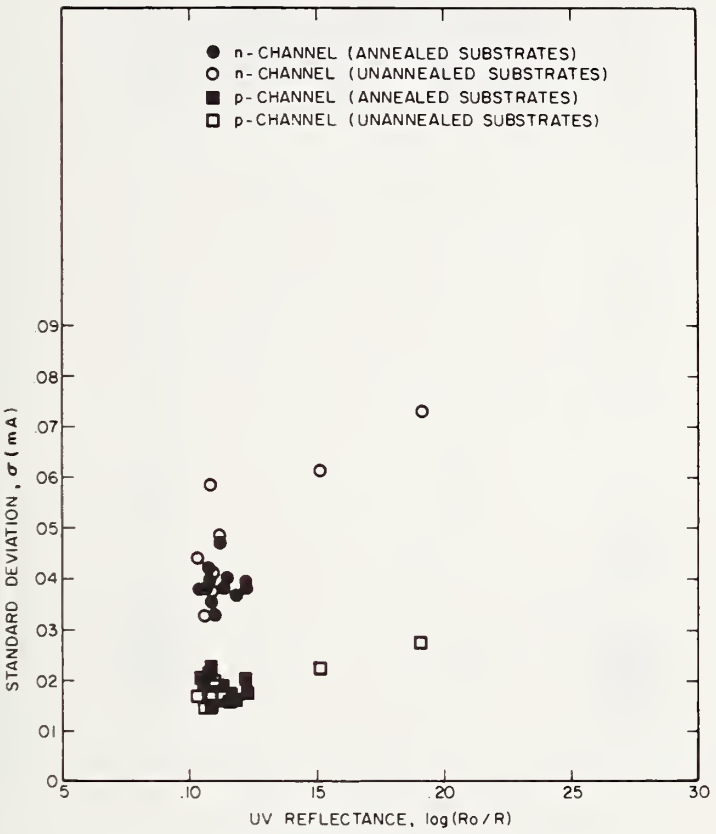

Figure 43. Plot of standard deviation for I_D vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = |V_T| + 4$ V, silicon film thickness = 0.4 μm (see fig. 39).

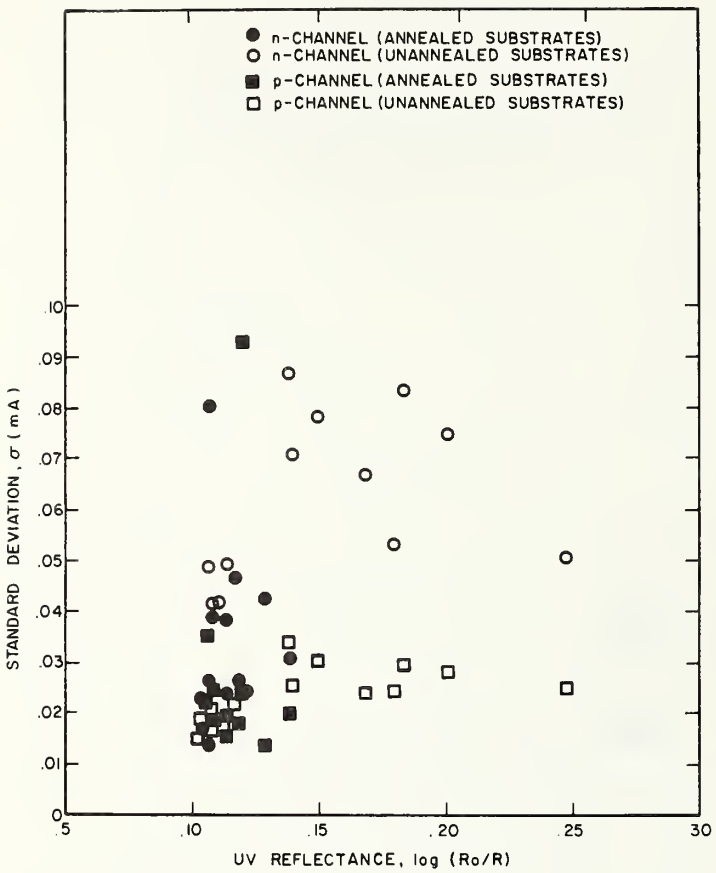

Figure 44. Plot of standard deviation for I_D vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 5$ V, silicon film thickness = 0.6 μm (see fig 40).

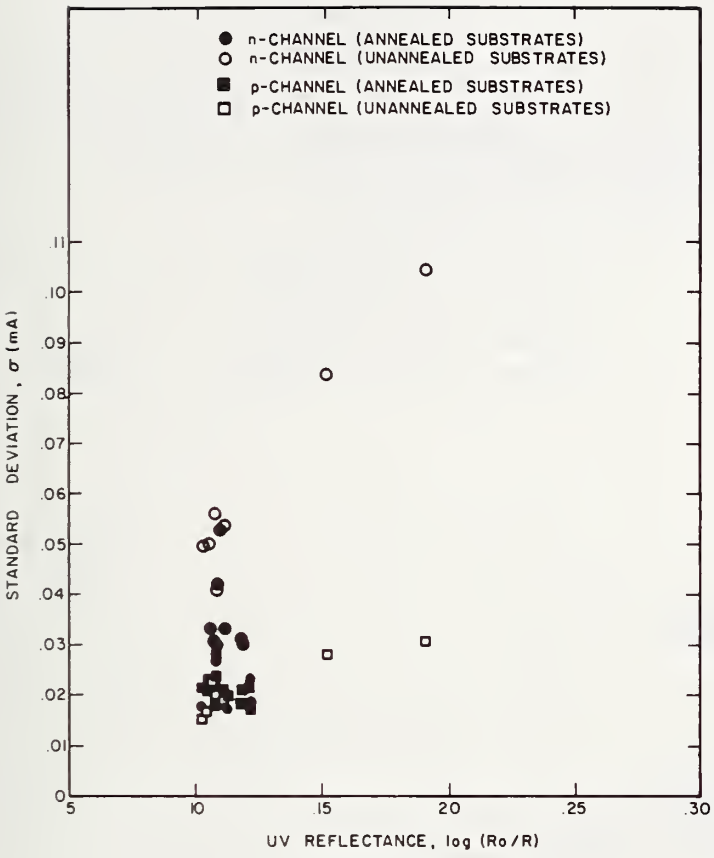

Figure 45. Plot of standard deviation for I_D vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 5$ V, silicon film thickness = 0.4 μm (see fig. 41).

Extrapolated threshold voltage, V_T, is plotted vs ultraviolet reflectance in figures 46 and 47. The values of V_T for devices on annealed substrates are clustered at low reflectance ratios, while V_T increases with decreasing film quality in the case of unannealed substrates. Substrate annealing also influences the magnitude of V_T for p-channel devices at low values of the ultraviolet reflectance term. The magnitude of V_T also depends on film thickness, increasing with increasing film thickness in the case of n-channel devices, and decreasing with increasing film thickness in the case of p-channel devices.

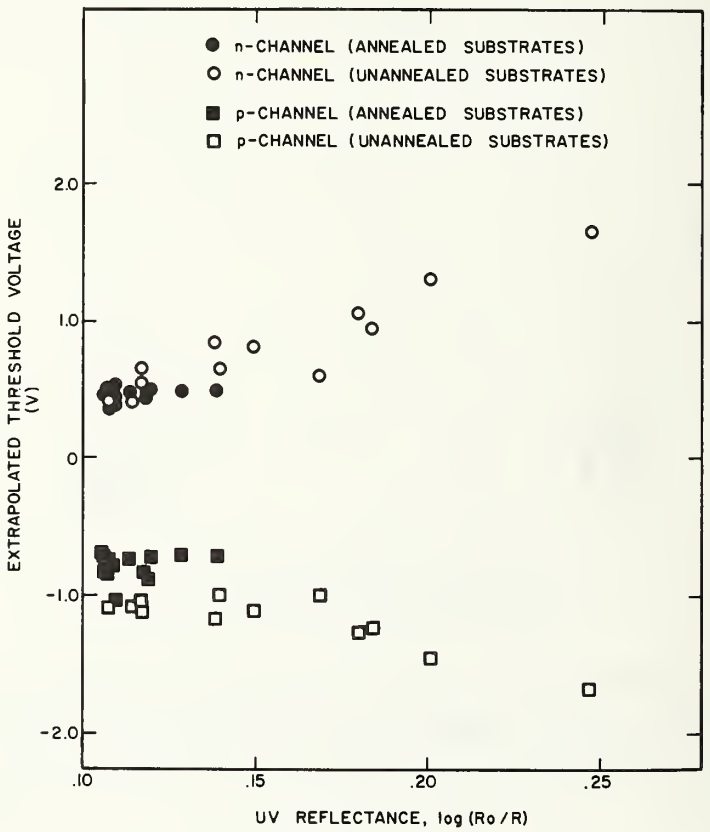

Figure 46. Plot of extrapolated threshold voltage, V_T, vs ultraviolet reflectance, silicon film thickness = 0.6 μm.

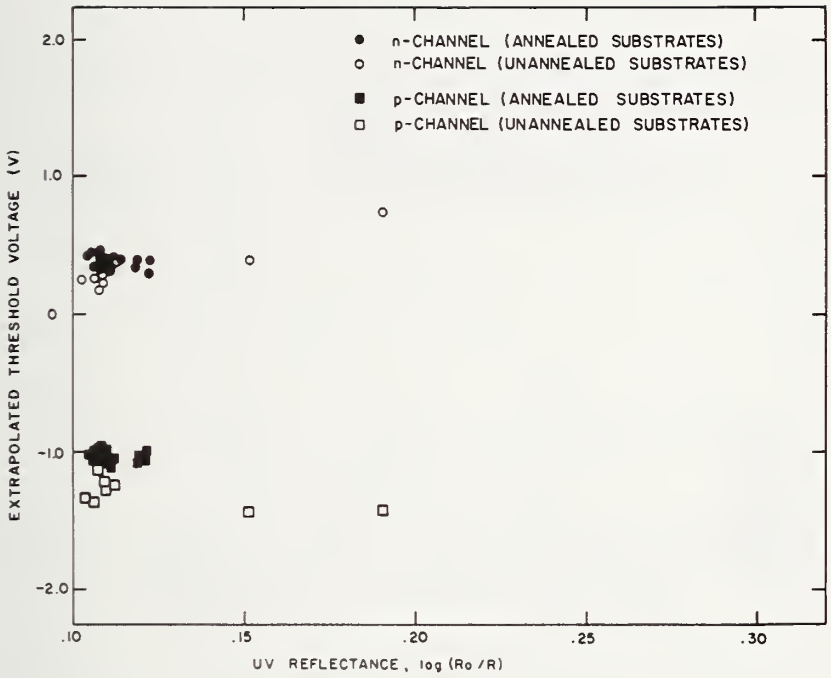

Figure 47. Plot of extrapolated threshold voltage, V_T, vs ultraviolet reflectance, silicon film thickness = 0.4 μm.

The standard deviation for V_T is shown in figures 48 and 49. At low ultraviolet values (which is the region of practical interest) the values of σ are lower for devices on annealed substrates, the thicker films (fig. 48) generally give rise to less spread in σ than the thinner films (fig. 49).

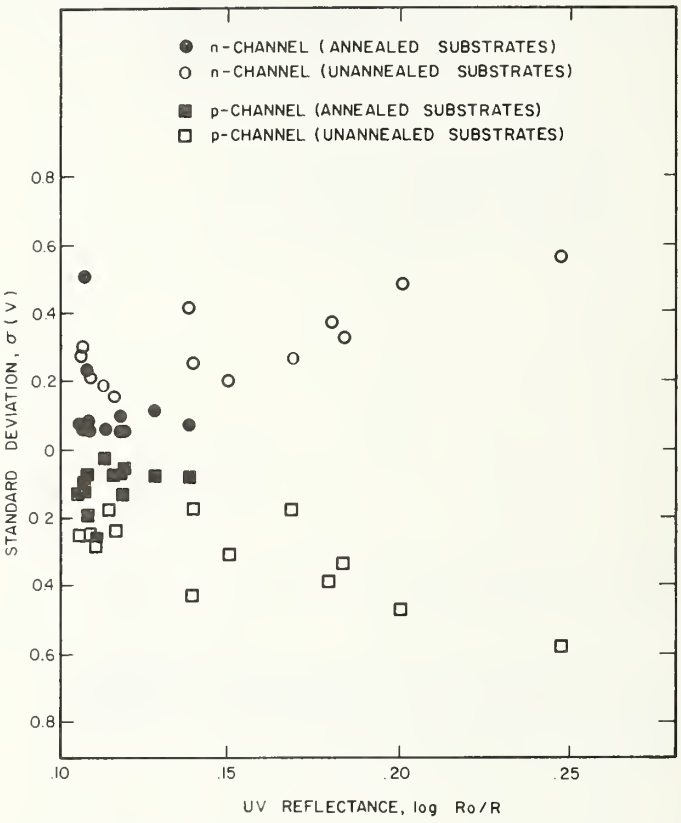

Figure 48. Plot of standard deviation for V_T vs ultraviolet reflectance, silicon film thickness = 0.6 μm (see fig. 46).

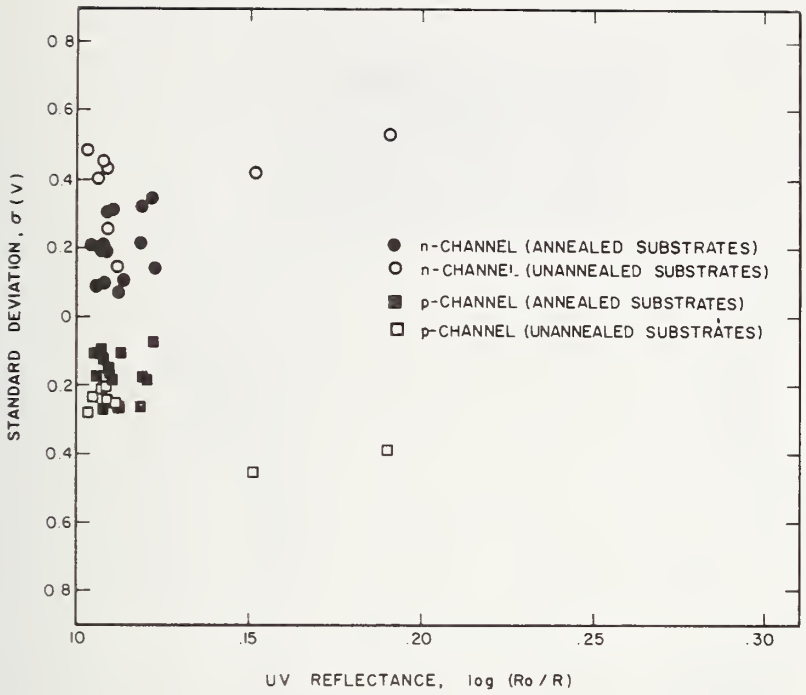

Figure 49. Plot of standard deviation for V_T vs ultraviolet reflectance, silicon film thickness = 0.4 μm (see fig. 47).

Leakage current vs ultraviolet reflectance is shown in figures 50 through 53. There is considerable scatter in the data indicating that other factors besides film quality are involved in determining leakage current. Leakage current for n-channel devices (at $V_G = 0$) on unannealed substrates increases as the silicon film quality improves, whereas it decreases in the case of p-channel devices. As indicated previously, gate biasing under "off" conditions ($|V_G| = 2$ V) results in little change in the leakage current of p-channel devices, but results in a reduction by about two orders of magnitude in the leakage current of n-channel devices. There are no indications, however, that degraded film quality, arising from substrate polishing damage, results in an increase in leakage current from a practical point of view.

The values of σ for leakage current are not given here since the observed trends are similar to those shown in figures 28 through 31. At low values of the ultraviolet reflectance term (high infrared ratios) there are no major differences between the σ values for devices on annealed and unannealed substrates.

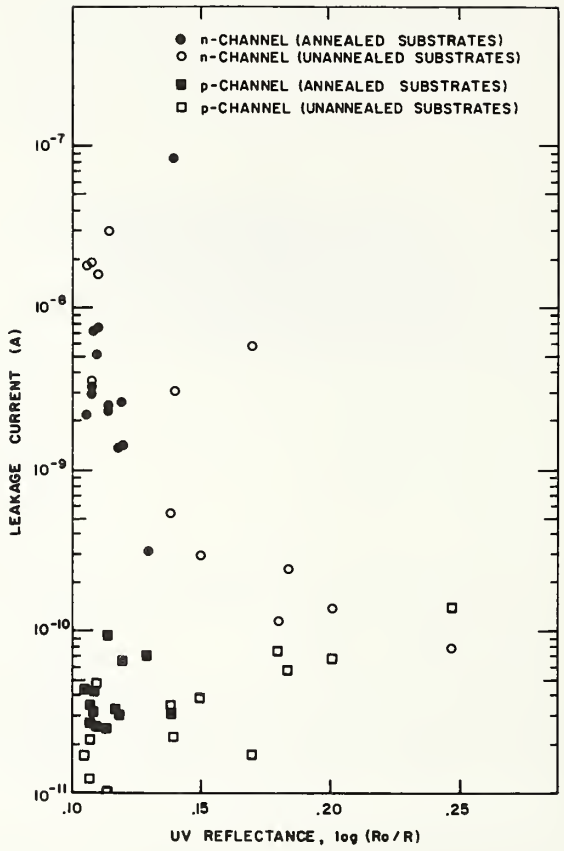

Figure 50. Plot of leakage current, I_L, vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.6 μm.

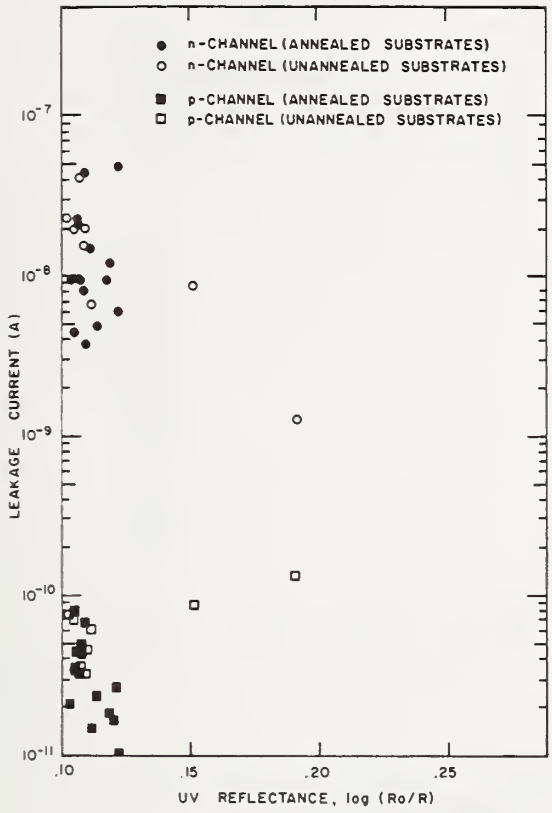

Figure 51. Plot of leakage current, I_L, vs ultraviolet reflectance, transistor biasing conditions: $|V_D| = 5$ V, $|V_G| = 0$ V, silicon film thickness = 0.4 μm.

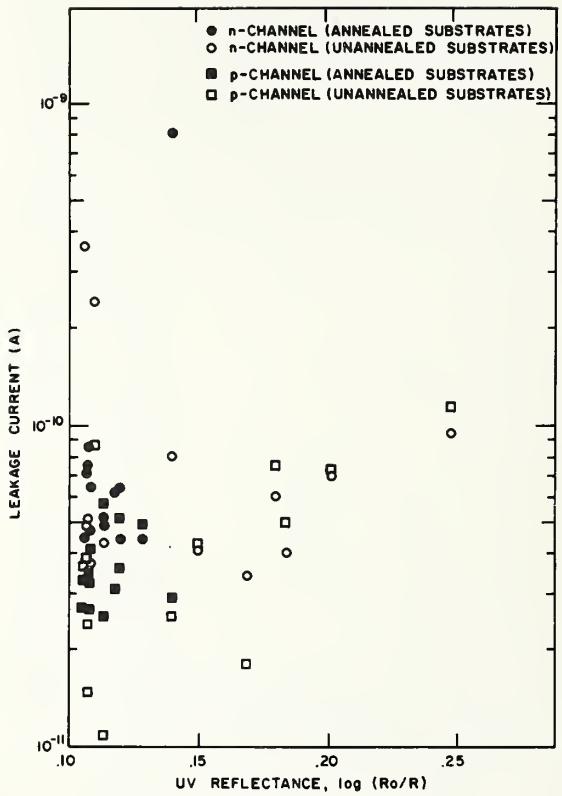

Figure 52. Plot of leakage current, I_L, vs ultraviolet reflectance, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = 2 V in the "off" condition for both transistor types, silicon film thickness = 0.6 μm.

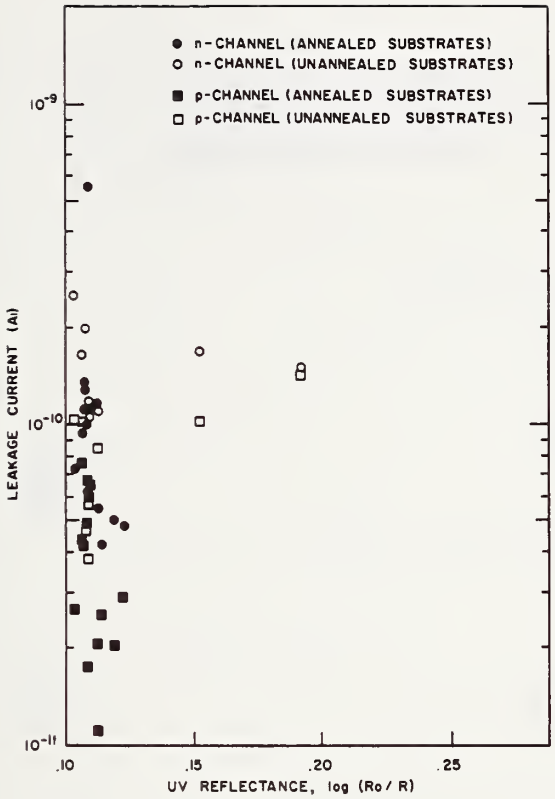

Figure 53. Plot of leakage current, I_L, vs ultraviolet reflectance, transistor biasing conditions: $|V_D|$ = 5 V, $|V_G|$ = 2 V in the "off" condition for both transistor types, silicon film thickness = 0.4 μm.

Drain breakdown voltage V_{BV}, as a function of ultraviolet reflectance, is shown in figures 54 and 55. The breakdown voltage for n-channel devices is lower than for p-channel devices. Substrate annealing results in the lowering of breakdown voltage values for both n- and p-channel devices fabricated in 0.6-μm-thick films. This effect is not observed in the case of devices fabricated in 0.4-μm-thick films.

The standard deviation for breakdown voltage is not shown since this information can be inferred from figures 34 and 35. There is little

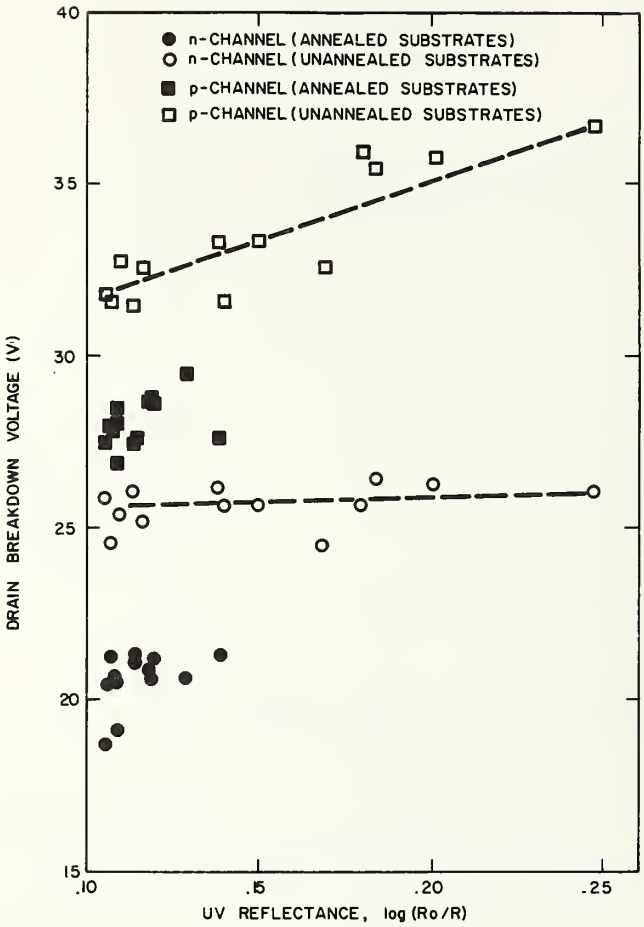

Figure 54. Plot of drain breakdown voltage, V_{BV}, vs ultraviolet reflectance, transistor biasing condition: $|V_G| = 2$ V in the "off" condition (I_D = 10 μA), silicon film thickness = 0.6 μm.

difference in the standard deviations observed for the different sets of devices fabricated in films characterized by low values of the ultraviolet reflectance parameters.

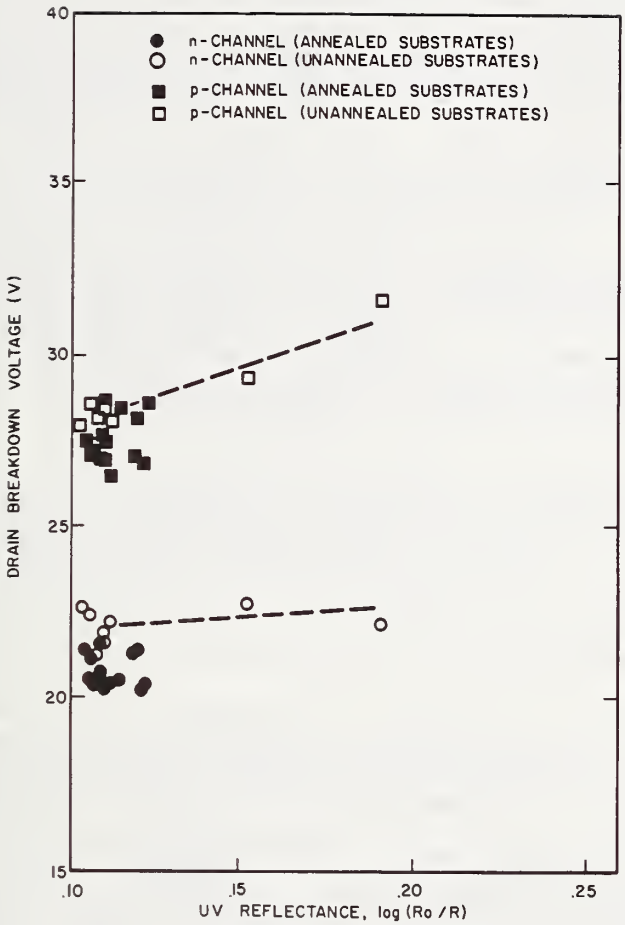

Figure 55. Plot of drain breakdown voltage, V_{BV}, vs ultraviolet reflectance, transistor biasing condition: $|V_G| = 2$ V in the "off" condition ($I_D = 10$ μA), silicon film thickness = 0.4 μm.

4. SUMMARY AND CONCLUSIONS

Infrared multiple reflectance provides a fast, nondestructive and sensitive means of quantitatively determining small changes in the surface quality of polished sapphire surfaces. However, if the sapphire is annealed prior to measurement, the reflectance method is insensitive to the initial level of damage or strain in the surface. This is due to the removal of lattice-related strain during the annealing process.

The comparison of infrared multiple-reflectance data with SOS discrete device performance reveals that there is an allowable range of substrate damage which does not impair device performance. The evaluation criteria were drain current (or field-effect mobility), threshold voltage, leakage current, and drain-breakdown voltage. Mean values and standard deviations were taken into account. The results also indicate that, based on the same criteria, there is a wide range of substrate surface damage which can be tolerated if substrates are annealed prior to silicon heteroepitaxy. It is interesting to note that both device performance and infrared reflectance are relatively insensitive to the initial substrate surface condition after the substrates are annealed. In general, device performance on damaged, but annealed, substrates was found to be superior to device performance on well-polished unannealed substrates. Thus, it appears that, for SOS device purposes, substrate annealing is more important than good surface polishing.

Ultraviolet reflectance provides a fast, nondestructive means of quantitatively determining the surface quality of silicon. The measurement method described in the text is sensitive to both surface crystallinity and surface texture which results in light-scattering effects. These are important considerations in the surface characterization of silicon on sapphire.

The results of ultraviolet reflectance measurements on silicon films (deposited on variously polished sapphire substrates) have been correlated with the results of infrared reflectance measurements on the corresponding substrates. The results have also been correlated with data from x-ray analysis and with SOS discrete device performance. The observed trends are as follows. There is an allowable range of substrate damage in unannealed substrates which has relatively little effect on film quality as determined by ultraviolet reflectance. There is a wide range of substrate surface damage which has little effect on film quality if substrates are annealed prior to silicon heteroepitaxy. These trends are similar to those discussed above for the dependence of device performance on substrate surface quality, thus, suggesting a correlation between the results of ultraviolet reflectance measurements and device performance. In general, device performance, based on the previous criteria, improves with improved film quality (as determined by ultraviolet reflectance). Thus, it may be concluded that substrate polishing is not the limiting factor in determining film quality and device performance.

Ultraviolet reflectance measurements have been used also for the detection of polishing damage in bulk silicon substrates as discussed in reference [17].

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

Specular reflectance measurements were used in the quantitative characterization of sapphire and silicon surfaces. Residual polishing damage in sapphire surfaces can be easily detected by infrared multiple reflectance measurements in the lattice-band region of sapphire, nominally 300 to 900 cm^{-1}. Specular reflectance measurements in the ultraviolet, at a photon energy of 4.3 eV (corresponding to the $X_4 - X_1$ silicon transition), have been used for the surface characterization of bulk silicon surfaces and silicon films on sapphire. This measurement is sensitive to crystalline quality, polishing damage, and surface texture which cause light-scattering effects. The reflectance methods are fast, nondestructive, and can be used for quality control and research purposes.

The reflectance methods were applied to the characterization of variously polished sapphire surfaces and to the characterization of heteroepitaxial silicon films grown on the substrates. The results of these measurements were correlated with various parameters of silicon-on-sapphire (SOS) devices fabricated in the silicon films. Measured device parameters include drain current, extrapolated threshold voltage, leakage current, and drain breakdown voltage. Most device data were automatically recorded using a special device test pattern and simple statistical data were computed for the various device parameters.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Infrared reflectance; optical reflectance; polishing; silicon on sapphire; surface roughness; ultraviolet reflectance; work damage.

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